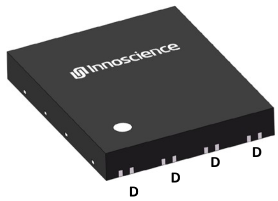
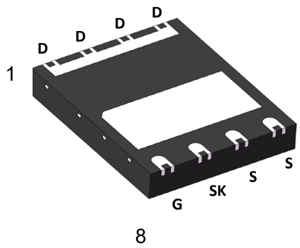
INN650DA150A

1. General description

650V GaN-on-silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 5 mm × 6 mm size

2. Features





- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	150	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	3	nC
$I_{D,pulse}$	32	A
Q_{OSS} @ V_{DS} = 400 V	28	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1,2,3,4	7	5,6

Table 3 Ordering information

Type/Ordering Code	Package	Marking (Product Code)
INN650DA150A	DFN 5X6	INN65DA150A

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6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain source voltage	$V_{DS,max}$	-	-	650	V	V_{GS} = 0 V, I_D = 25 µA
Drain source voltage transient [1]	$V_{DS(transient)}$	-	-	750	V	V_{GS} = 0 V, V_{DS} = 750 V
Continuous current, drain source	I_D	-	-	17	A	T_c = 25 °C
Pulsed current, drain source [2]	$I_{D,pulse}$	-	-	32	A	T_c = 25 °C; V_G = 6 V; See Figure 16;
Pulsed current, drain source [2]	$I_{D,pulse}$	-	-	23	A	T_c = 125 °C;V_G = 6 V; See Figure 17;
Gate source voltage, continuous [3]	V_{GS}	-1.4	-	+7	V	T_j = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20	-	+10	V	T_j = -55 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz open drain
Power dissipation	P_{tot}	-	-	113	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	˚C	
Storage temperature	T_{stg}	-55	-	+150	˚C	

1 $V_{DS(transient)}$ is intended for surge rating during non-repetitive events, t_{PULSE} < 1 µs

2 Pulse = 300 µs

3 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	1.1	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.2	V	I_D = 17.2 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.5	-		I_D = 17.2 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	0.7	25	μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	6	200		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	30	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	115	150	mΩ	V_{GS} = 6 V; I_D = 5 A; T_j = 25 °C
		-	234	-	mΩ	V_{GS} = 6 V; I_D = 5 A; T_j = 150 °C
Gate resistance	R_G	-	1.4	-	Ω	f = 5 MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	110	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	30	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.46	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	42	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	68	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{oss}	-	28	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	3	-	nS	See Figure 22
Turn-off delay time	$t_{d(off)}$	-	7	-	nS	See Figure 22
Rise time	t_r	-	5	-	nS	See Figure 22
Fall time	t_f	-	5	-	nS	See Figure 22

1 $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

2 $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	3	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D= 5 A
Gate-source charge	Q_{GS}	-	0.28	-	nC	
Gate-drain charge	Q_{GD}	-	1.63	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.3	-	V	V_{DS} = 400 V; I_D= 5 A

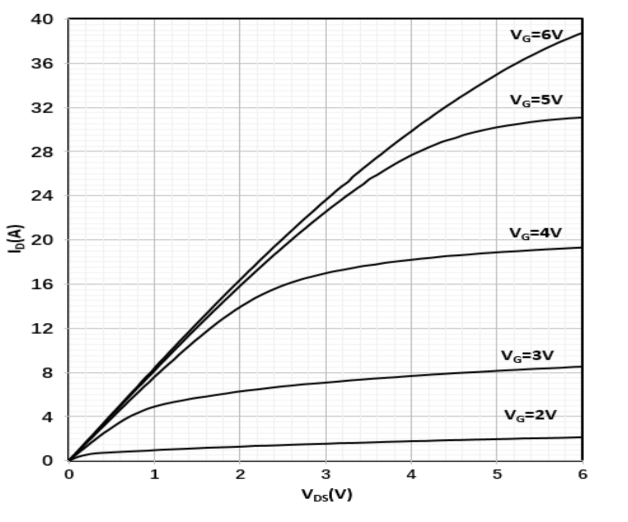
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.6	-	V	V_{GS} = 0 V; I_S = 5 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	32	A	V_{GS} = 6 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} = 5 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

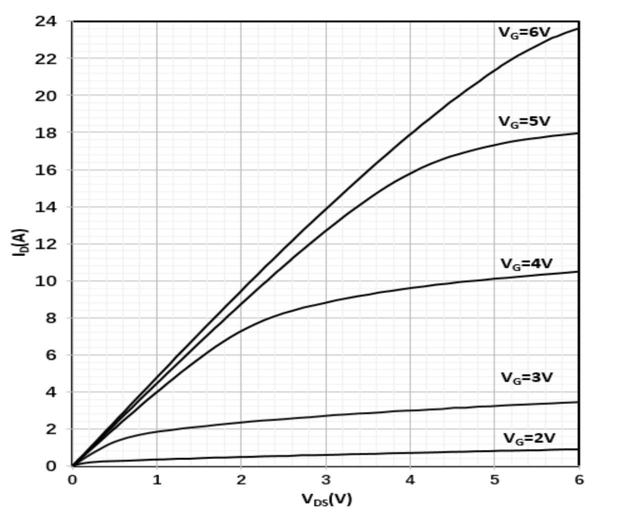
at T_j = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



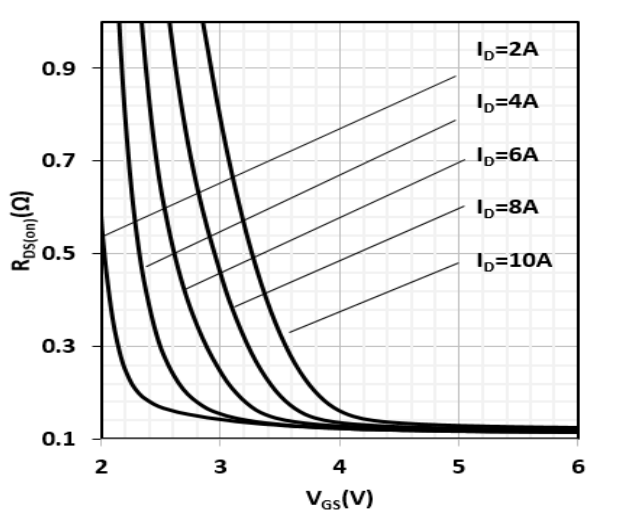
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



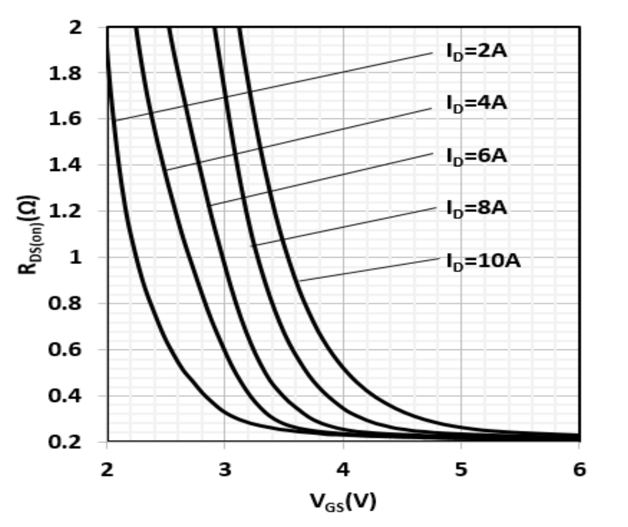
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance



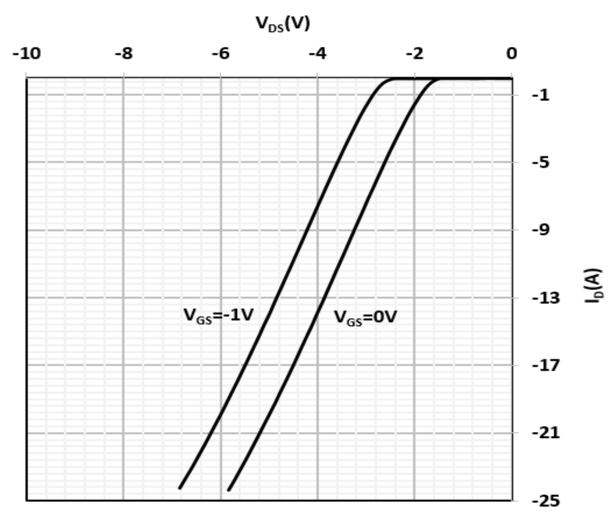
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 25 °C

Figure 4 Typ. Drain-source on-state resistance



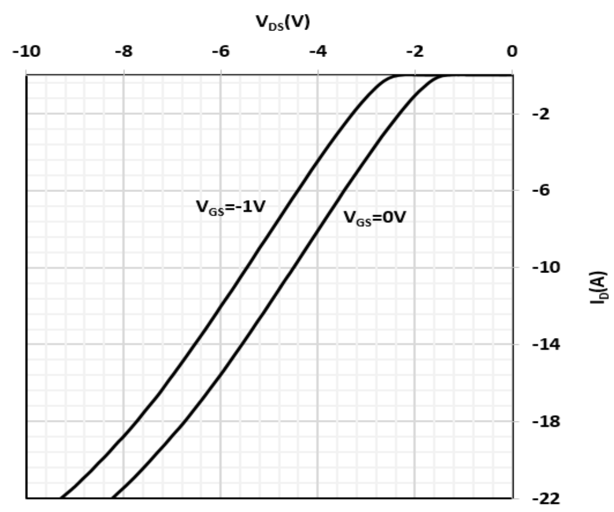
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



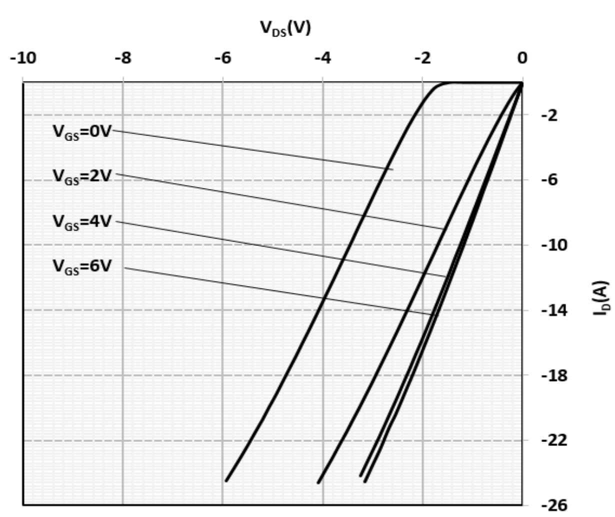
$I_D = f(V_{DS}, V_{GS})$; T_j= 25 °C

Figure 6 Typ. channel reverse characteristics



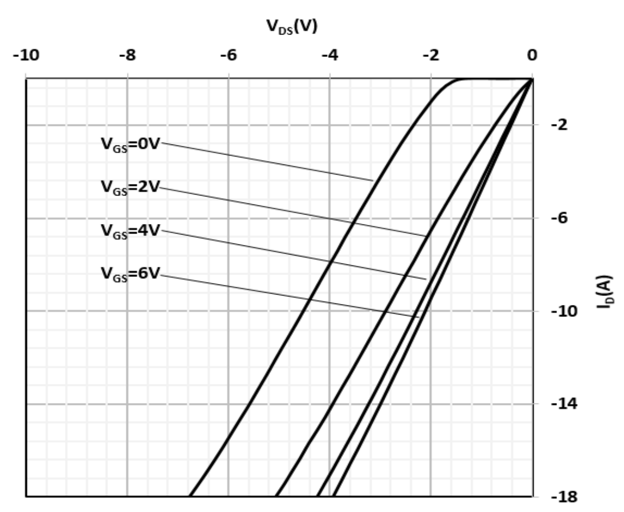
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 7 Typ. channel reverse characteristics



$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 8 Typ. channel reverse characteristics



$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

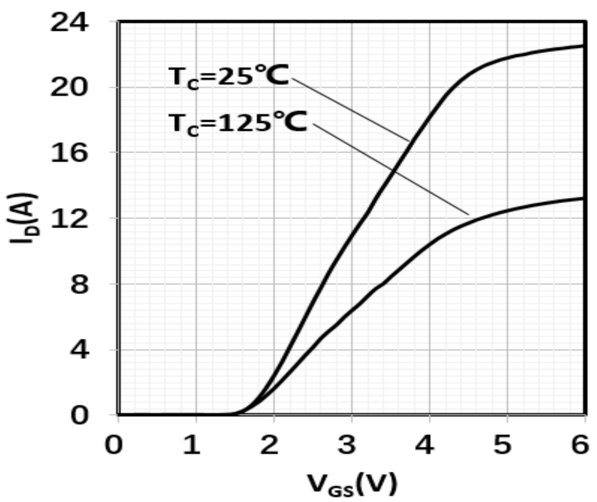
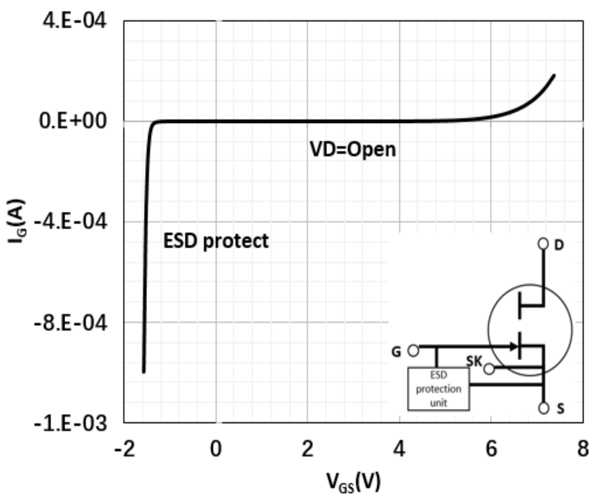
Figure 9 Typ. transfer characteristics	Figure 10 Typ. Gate-to-Source leakage
	
$I_D = f(V_{GS})$; V_{DS}= 3 V	$I_G = f(V_{GS})$; Ig reverse turn on by ESD unit

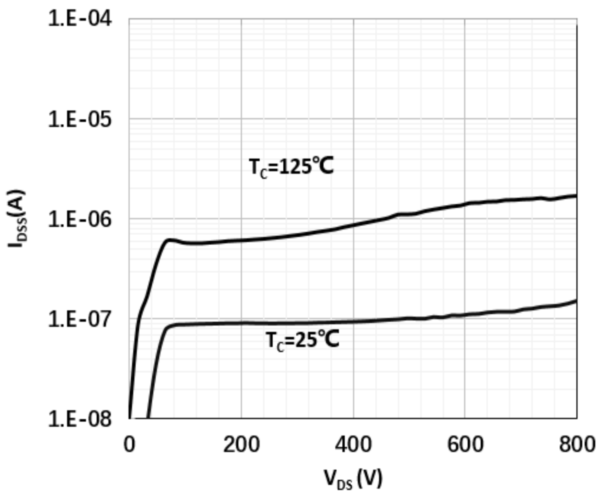
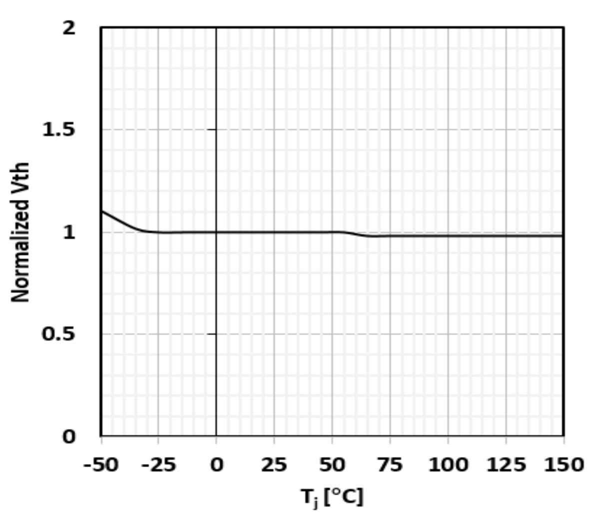
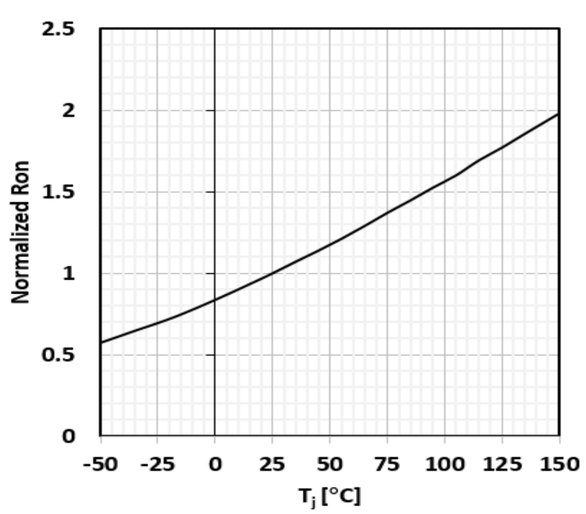
Figure 11 Drain-source leakage characteristics

$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

Figure 12 Gate threshold voltage



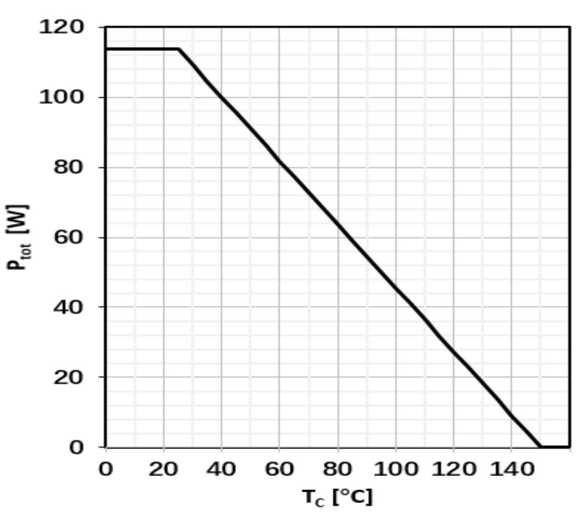
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 17.2 mA

Figure 13 Drain-source on-state resistance



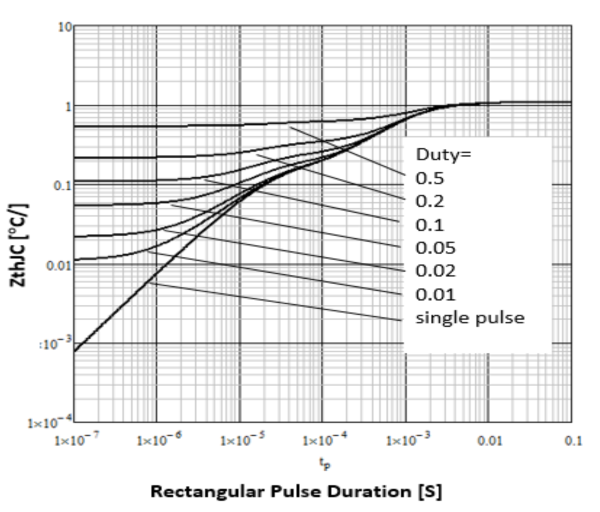
$R_{DS(on)} = f(T_j)$; I_D = 5 A; V_G=6V

Figure 14 Power dissipation



$P_{tot} = f(T_C)$

Figure 15 Max.transient thermal impedance



$Z_{thJC} = f(t_P, D)$

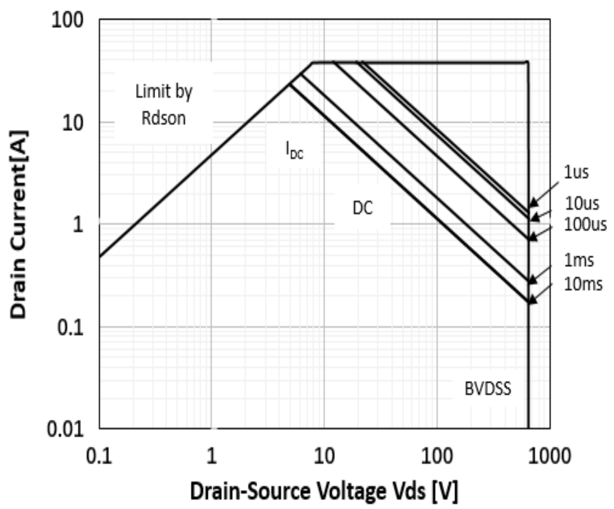
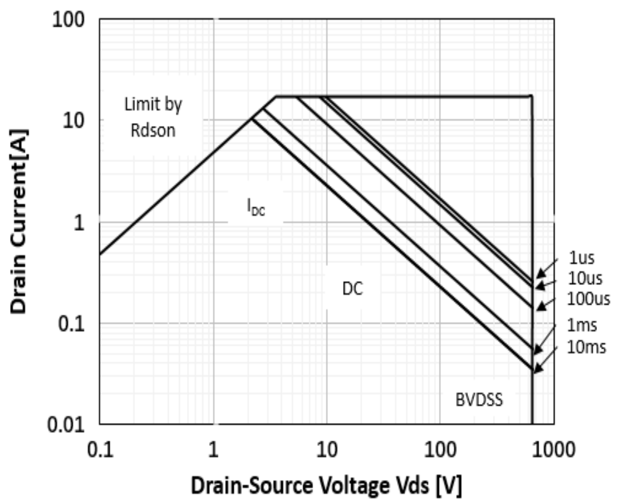
Figure 16 Safe operating area	Figure 17 Safe operating area
	
$I_D = f(V_{DS})$; T_C = 25 °C	$I_D = f(V_{DS})$; T_C = 125 °C

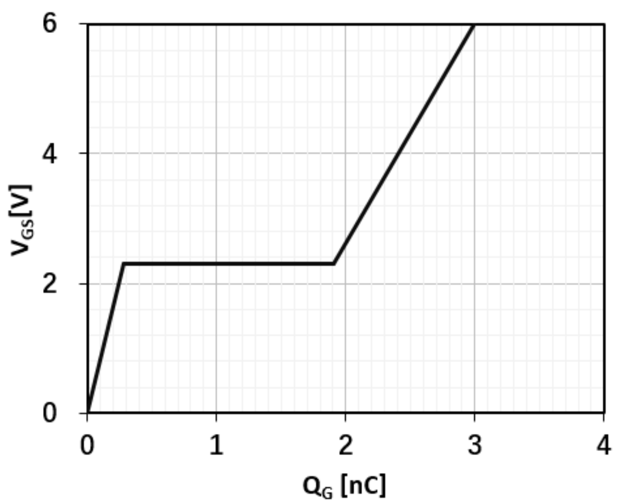
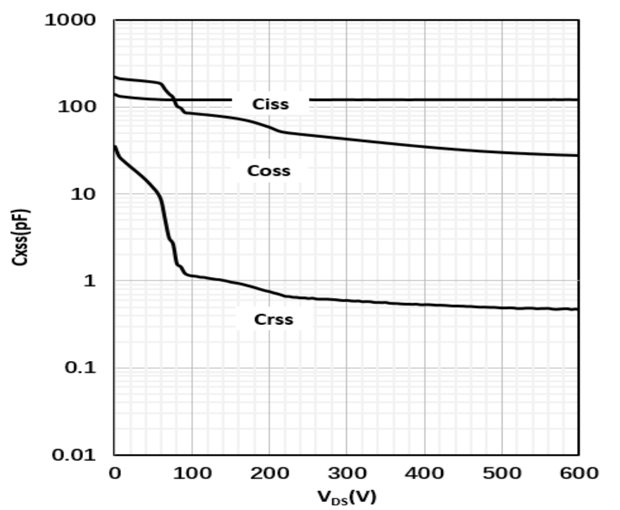
Figure 18 Typ. gate charge	Figure 19 Typ. capacitances
	
$V_{GS} = f(Q_G)$; V_{DCLINK}= 400 V; I_D = 5 A	$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

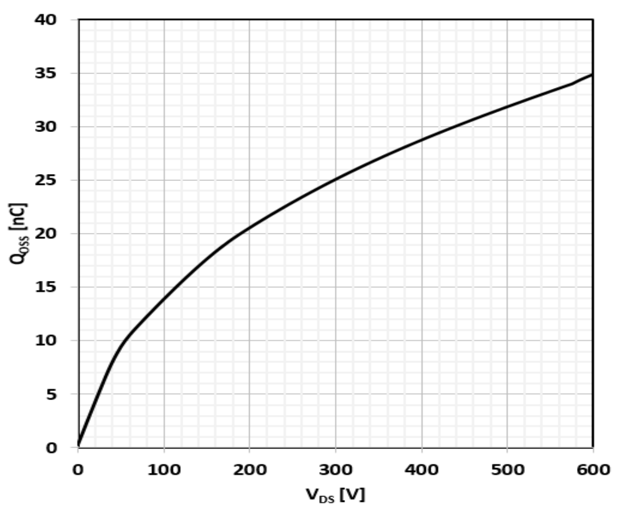
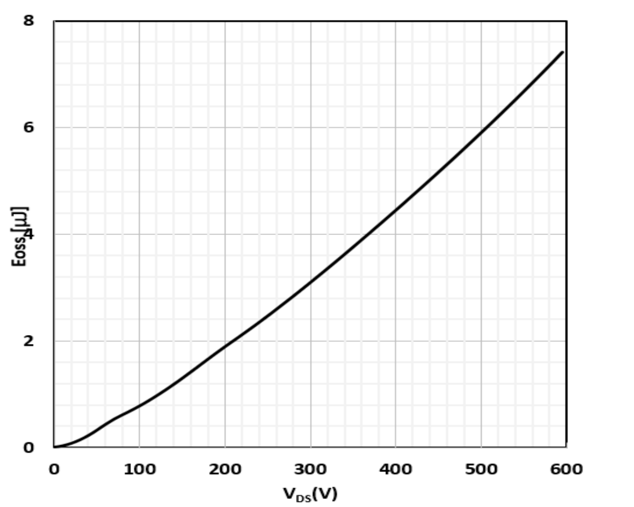
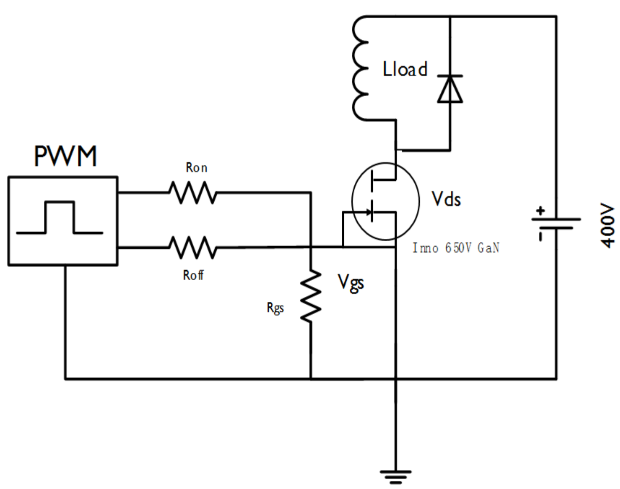
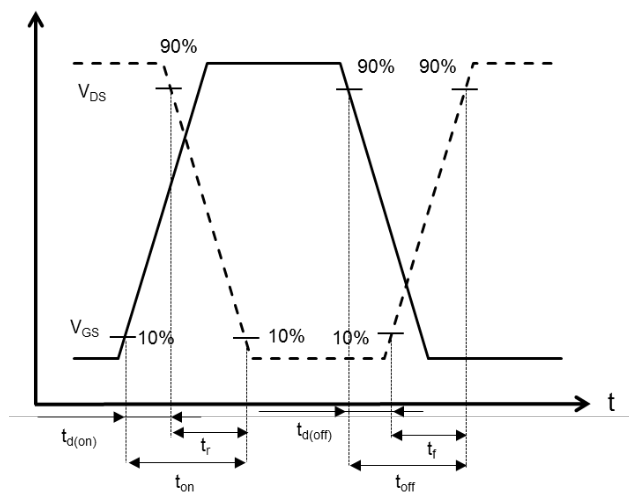
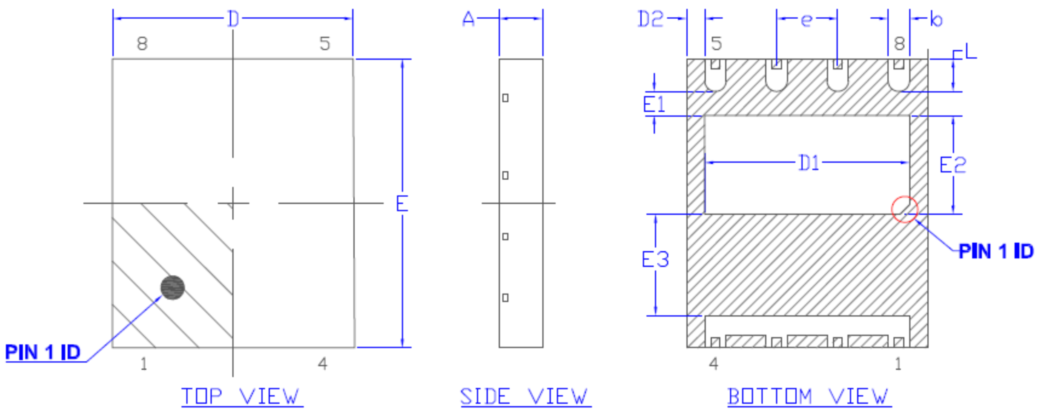
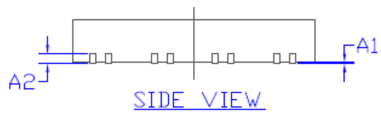
Figure 20 Typ. output charge	Figure 21 Typ. Coss stored Energy
	
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz	$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 22 Typ.Switching times with inductive load	Figure 23 Typ.Switching times waveform
	
V_{DS}=400V, I_D=5A, L_{load}=800uH, V_{GS}=6V, R_{on}=10Ω, R_{off}=2Ω, R_{gs}=10kΩ	

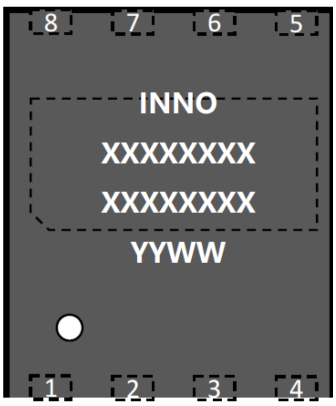
10.Package outlines





SYMBOL	DIMENSION			SYMBOL	DIMENSION		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.80	0.90	1.00	E	6.00 B.S.C		
A1	0.00	0.02	0.05	E1	0.40	0.50	0.60
A2	---	0.203 ref	---	E2	1.95	2.05	2.15
b	0.40	0.45	0.50	E3	---	2.10	---
D	5.00 B.S.C			e	1.27 B.S.C		
D1	4.16	4.26	4.36	L	0.575	0.675	0.775
D2	0.27	0.37	0.47				

Notes:
(1) Dimension and tolerance conform to ASME Y14.5-2009.
(2) All dimensions are in millimeters.
(3) Lead coplanarity shall be 0.1 millimeters max.
(4) Complies with JEDEC MO-229.
(5) Drawing is not to scale.



Row	Description	Example
Row 1	Company name	INNO
Row 2	Product code (In short)	XXXXXXXX
Row 3	ASSY lot No.	XXXXXXXX
Row 4	Date code	YYWW

11. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2021-4-26	1.0 version release

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