

INN650D260A

1. General description

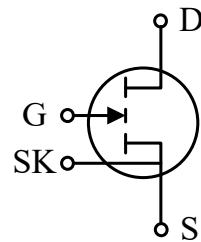
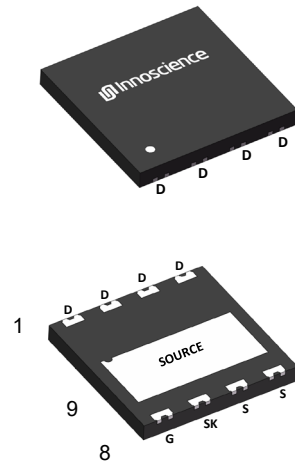
650V GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 8 mm × 8 mm size

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion



4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^{\circ}\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max} @ V_{GS} = 6\text{ V}$	260	mΩ
$Q_{G,typ} @ V_{DS} = 400\text{ V}$	2	nC
$I_{D,pulse}$	22	A
$Q_{OSS} @ V_{DS} = 400\text{ V}$	19	nC
$Q_{rr} @ V_{DS} = 400\text{ V}$	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1,2,3,4	7	5,6,9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN650D260A	DFN 8X8	65D260A

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6. Maximum ratings

at $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain source voltage	$V_{DS,max}$	-	-	650	V	$V_{GS} = 0\text{ V}$, $T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Drain source voltage transient ¹	$V_{DS(transient)}$	-	-	800	V	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$
Drain source voltage, pulsed ²	$V_{DS,surge}$			750	V	$T_j = 25\text{ }^{\circ}\text{C}$; total time < 10h
Drain source voltage, pulsed ²	$V_{DS,surge}$			750	V	$T_j = 125\text{ }^{\circ}\text{C}$; total time < 1h
Continuous current, drain source	I_D	-	-	12	A	$T_c = 25\text{ }^{\circ}\text{C}$
Pulsed current, drain source ³	$I_{D,pulse}$	-	-	22	A	$T_c = 25\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; See Figure 16;
Pulsed current, drain source ³	$I_{D,pulse}$	-	-	15	A	$T_c = 125\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; See Figure 17;
Gate source voltage, continuous ⁴	V_{GS}	-1.4	-	+7	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Gate source voltage, pulsed	$V_{GS,pulse}$	-20	-	+10	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$ open drain
Power dissipation	P_{tot}	-	-	75	W	$T_c = 25\text{ }^{\circ}\text{C}$
Operating temperature	T_j	-55	-	+150	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	-55	-	+150	$^{\circ}\text{C}$	

1 $V_{DS(transient)}$ is intended for surge rating during non-repetitive events, $t_{PULSE} < 200\text{ }\mu\text{s}$

2 $V_{DS,surge}$ is intended for surge rating during repetitive pulse, $t_{PULSE} < 100\text{ ns}$

3 Pulse = 300 μs

4 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	1.65	°C/W	
Reflow soldering temperature	T_{sld}	-	-	260	°C	MSL3

8. Electric characteristics

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.2	V	$I_D = 11\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	1.9	-		$I_D = 11\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150\text{ }^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	-	2	20	μA	$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	10	120		$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	40	-	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	165	260	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 3\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	322	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 3\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate resistance	R_G	-	2	-	Ω	$f = 5\text{ MHz}$; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	73	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	20	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Reverse transfer capacitance	C_{rss}	-	0.2	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	27	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	43	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	19	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	3	-	nS	See Figure 22
Turn-off delay time	$t_{d(off)}$	-	4	-	nS	See Figure 22
Rise time	t_r	-	7	-	nS	See Figure 22
Fall time	t_f	-	4	-	nS	See Figure 22

1 $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

2 $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V}; I_D = 3 \text{ A}$
Gate-source charge	Q_{GS}	-	0.18	-	nC	
Gate-drain charge	Q_{GD}	-	0.62	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.3	-	V	$V_{DS} = 400 \text{ V}; I_D = 3 \text{ A}$

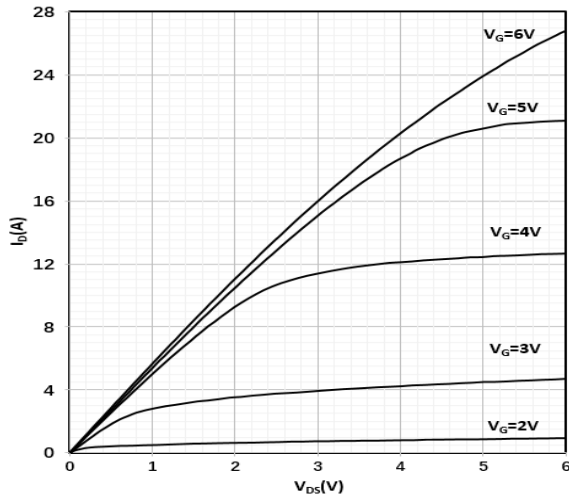
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.7	-	V	$V_{GS} = 0 \text{ V}; I_{SD} = 3 \text{ A}$
Pulsed current, reverse	$I_{S,pulse}$	-	-	22	A	$V_G = 6 \text{ V}$
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_{SD} = 3 \text{ A}; V_{DS} = 400 \text{ V}$
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

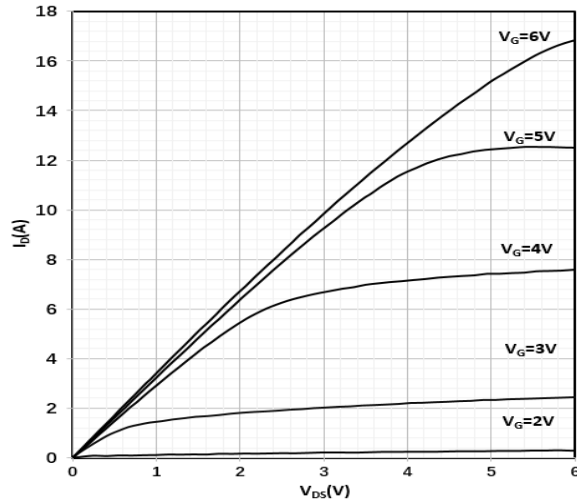
at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Figure 1 Typ. output characteristics



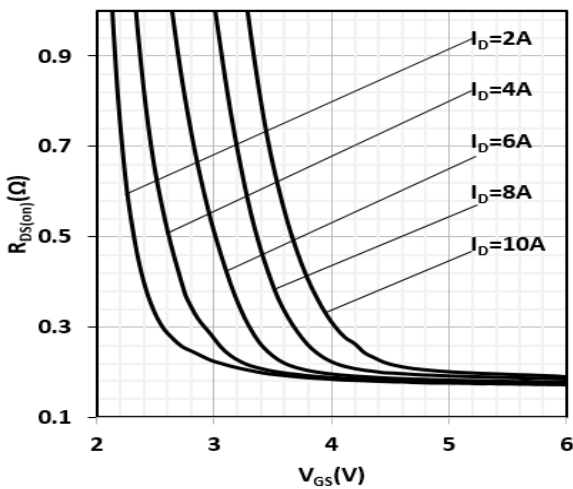
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

Figure 2 Typ. output characteristics



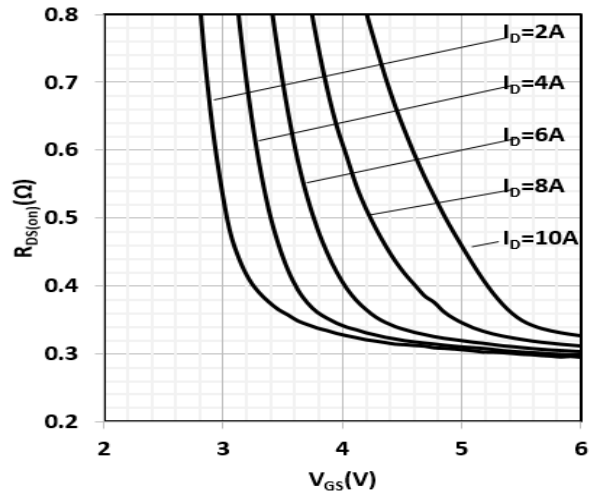
$$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 3 Typ. Drain-source on-state resistance



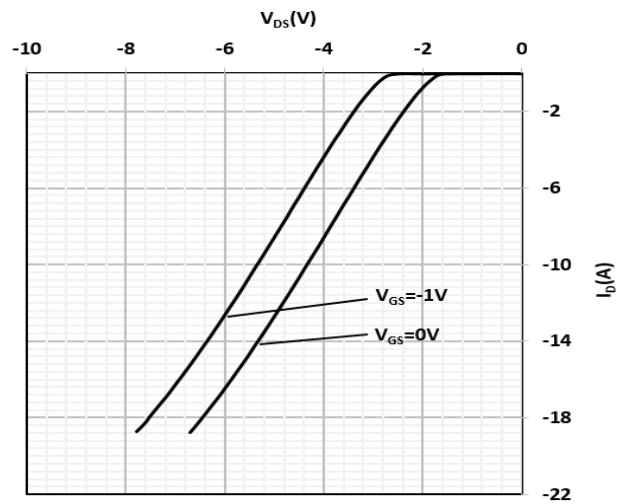
$$R_{DS(on)} = f(I_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

Figure 4 Typ. Drain-source on-state resistance



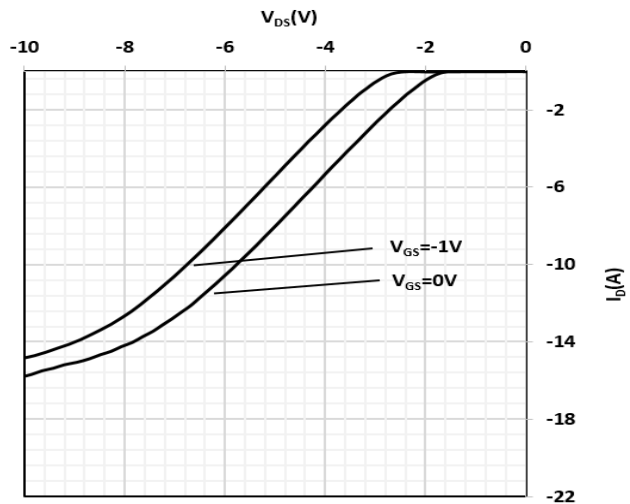
$$R_{DS(on)} = f(I_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 5 Typ. channel reverse characteristics



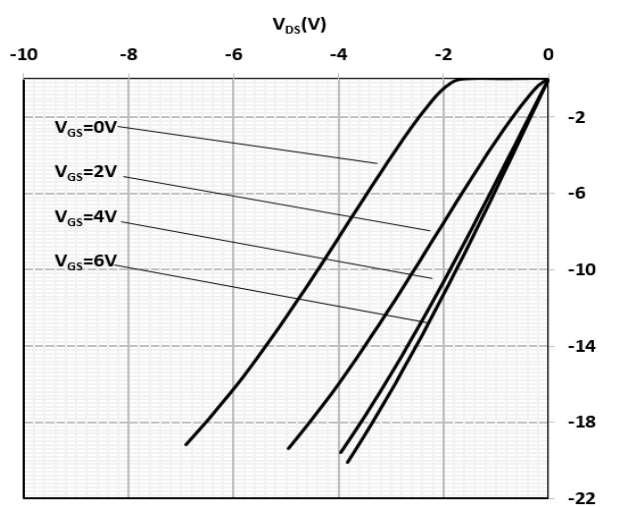
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$

Figure 6 Typ. channel reverse characteristics



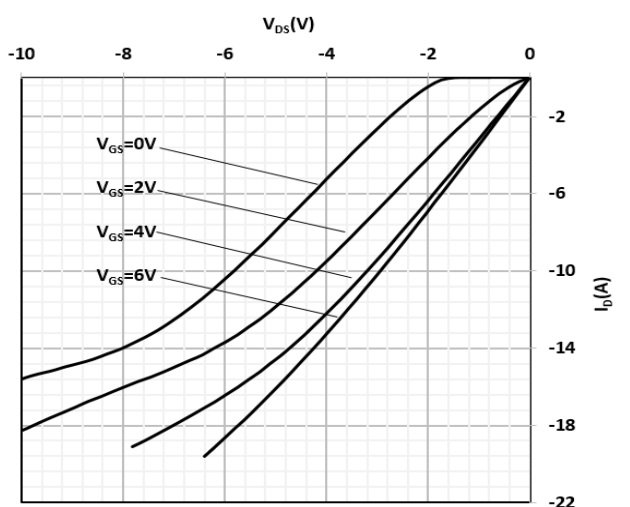
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$

Figure 7 Typ. channel reverse characteristics



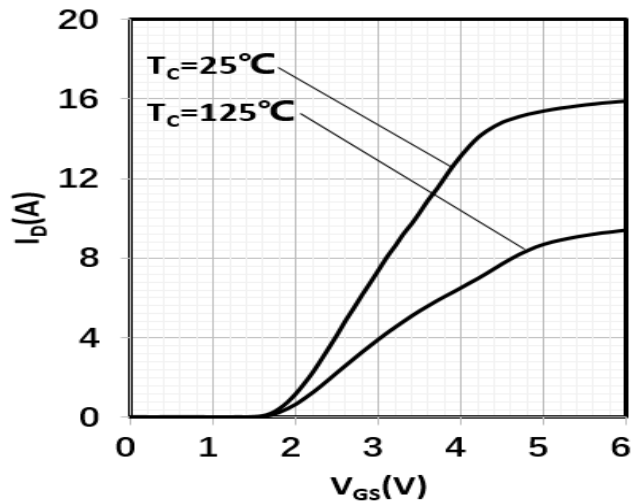
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$

Figure 8 Typ. channel reverse characteristics



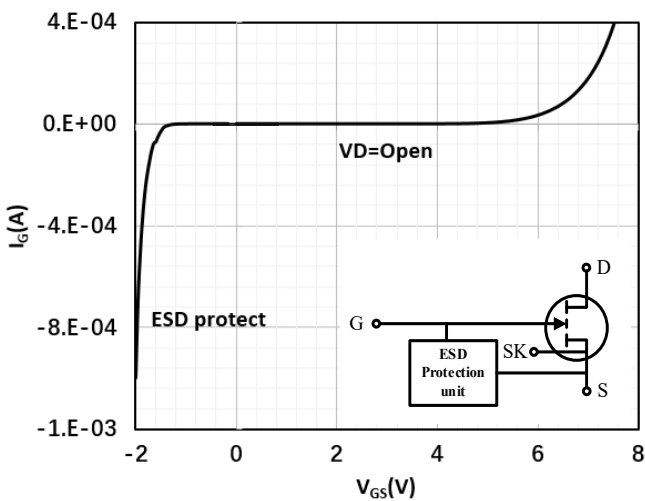
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$

Figure 9 Typ. transfer characteristics



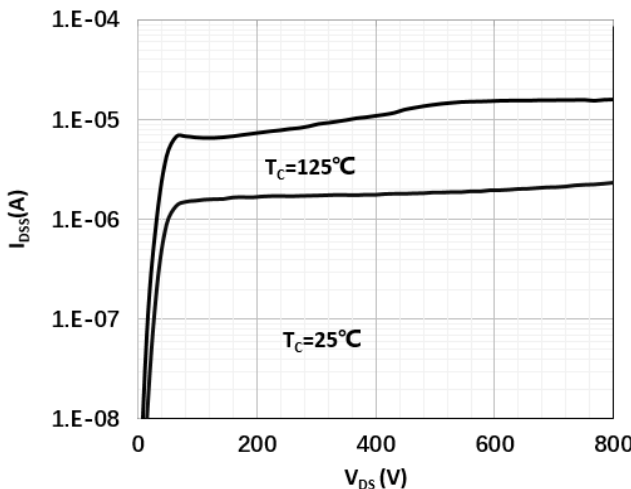
$I_D = f(V_{GS}); V_{DS} = 3 \text{ V}$

Figure 10 Typ. Gate-to-Source leakage



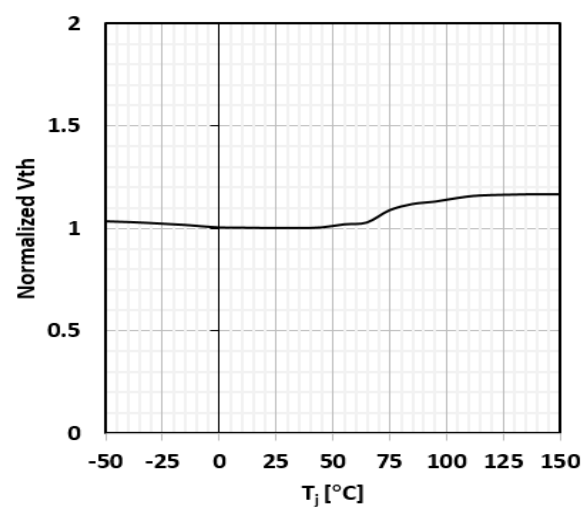
$I_G = f(V_{GS}); I_G$ reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



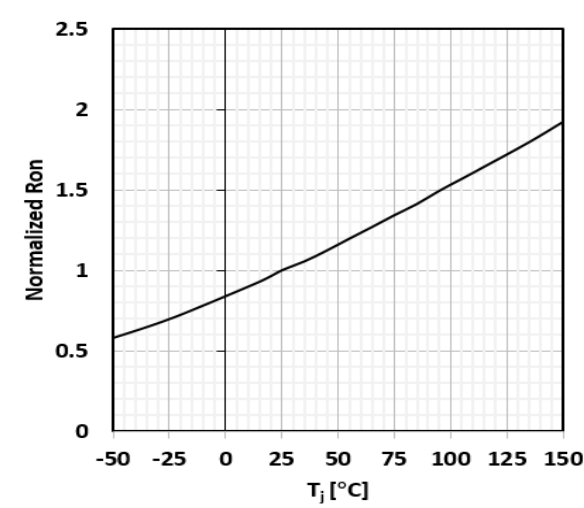
$I_{DSS} = f(V_{DS}); V_{GS} = 0 \text{ V}$

Figure 12 Gate threshold voltage



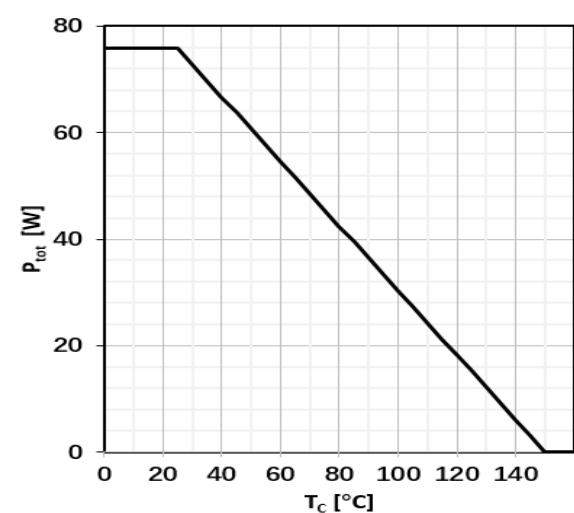
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 11\text{ mA}$

Figure 13 Drain-source on-state resistance



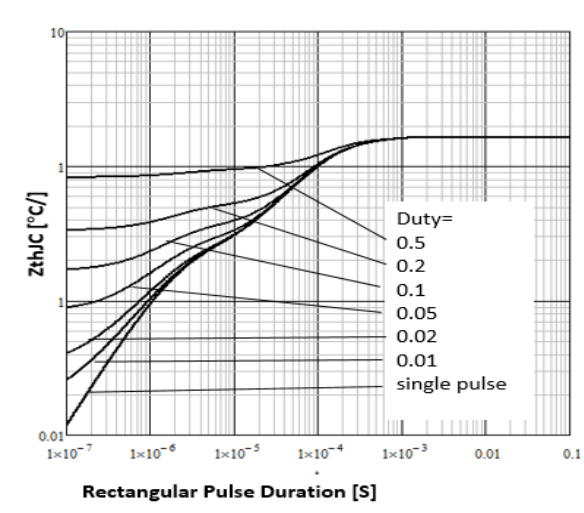
$R_{DS(on)} = f(T_j)$; $I_D = 3\text{ A}$; $V_G=6\text{ V}$

Figure 14 Power dissipation



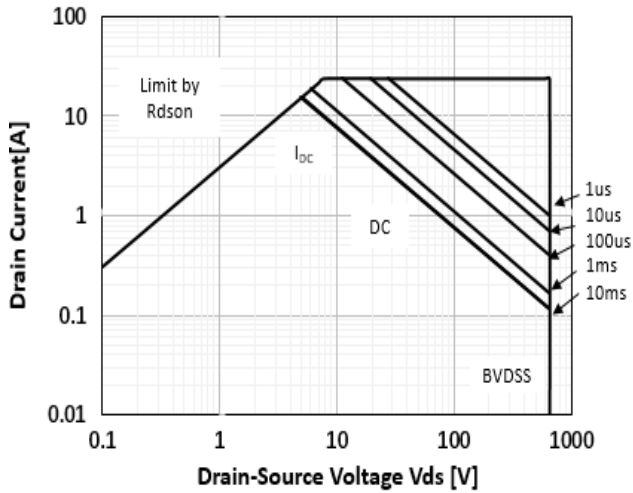
$P_{tot} = f(T_c)$

Figure 15 Max.transient thermal impedance



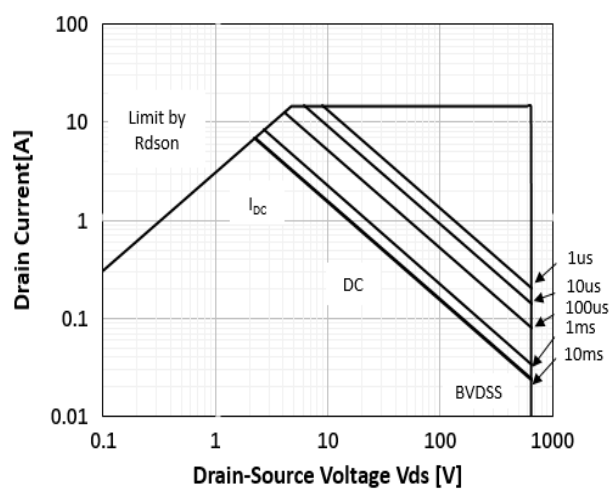
$Z_{thJC} = f(t_P, D)$

Figure 16 Safe operating area



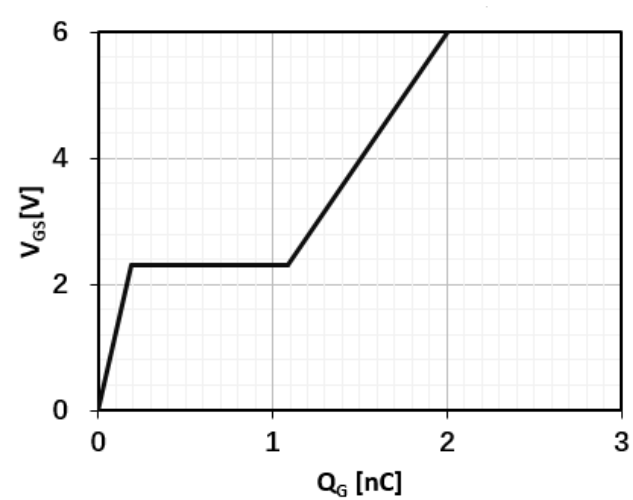
$$I_D = f(V_{DS}); T_C = 25\text{ }^{\circ}\text{C}$$

Figure 17 Safe operating area



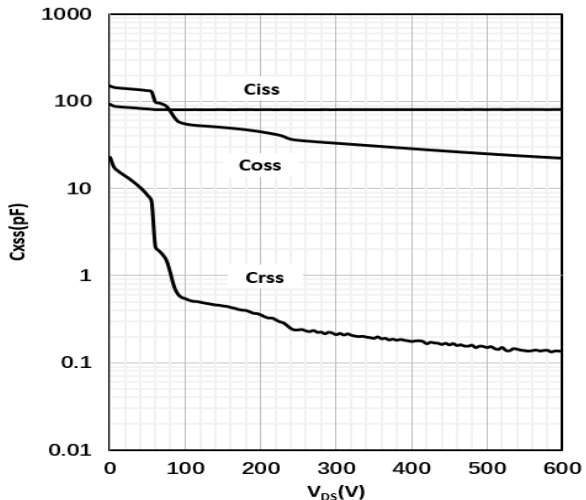
$$I_D = f(V_{DS}); T_C = 125\text{ }^{\circ}\text{C}$$

Figure 18 Typ. gate charge



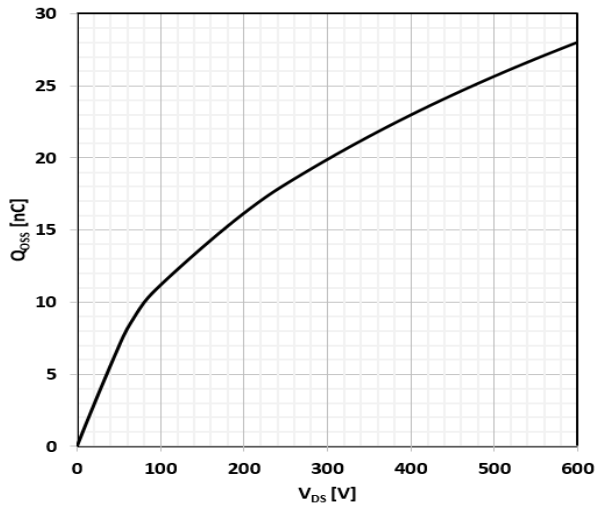
$$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 3\text{ A}$$

Figure 19 Typ. capacitances



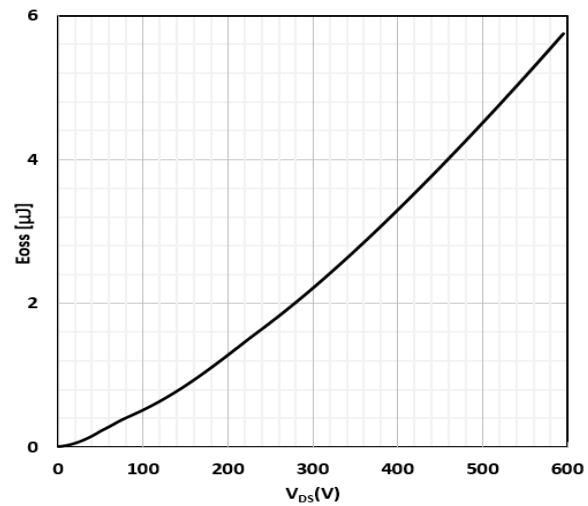
$$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$$

Figure 20 Typ. output charge



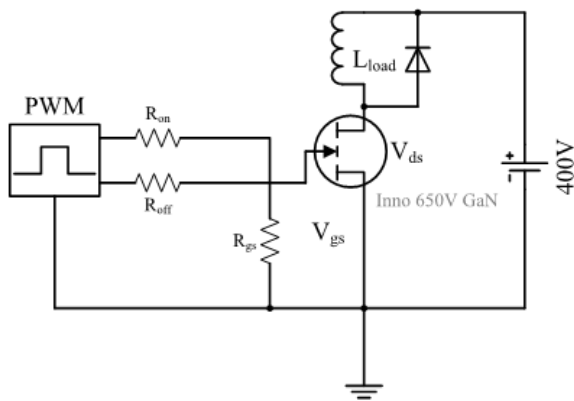
$$Q_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$$

Figure 21 Typ. Coss stored Energy



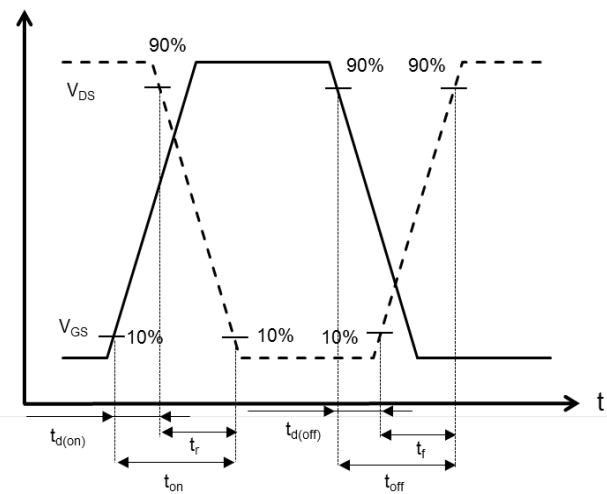
$$E_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$$

Figure 22 Typ. Switching times with inductive load

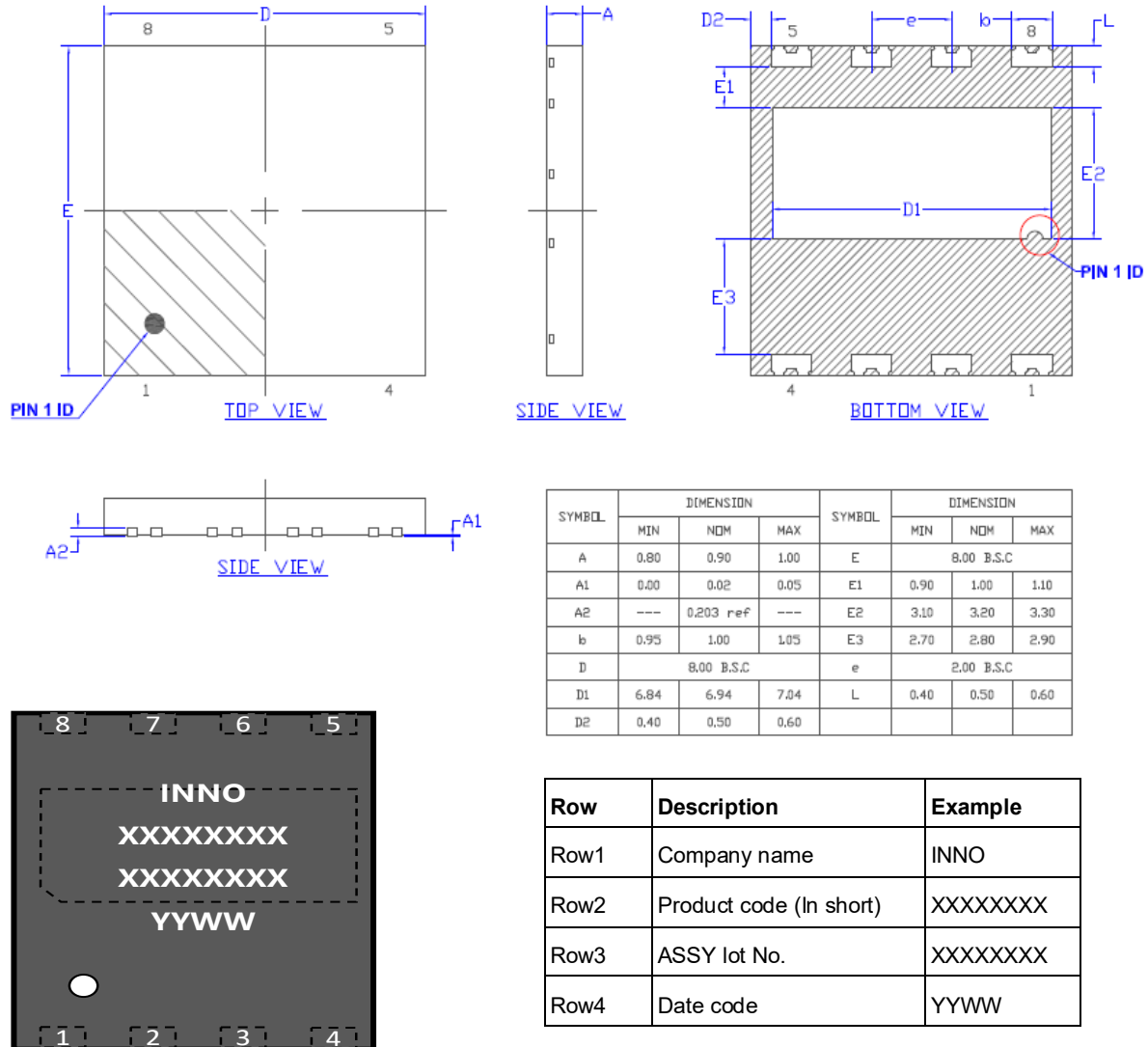


$V_{DS}=400\text{V}$, $I_D=5\text{A}$, $L_{load}=800\mu\text{H}$, $V_{GS}=6\text{V}$, $R_{on}=10\Omega$,
 $R_{off}=2\Omega$, $R_{gs}=10\text{k}\Omega$

Figure 23 Typ. Switching times waveform



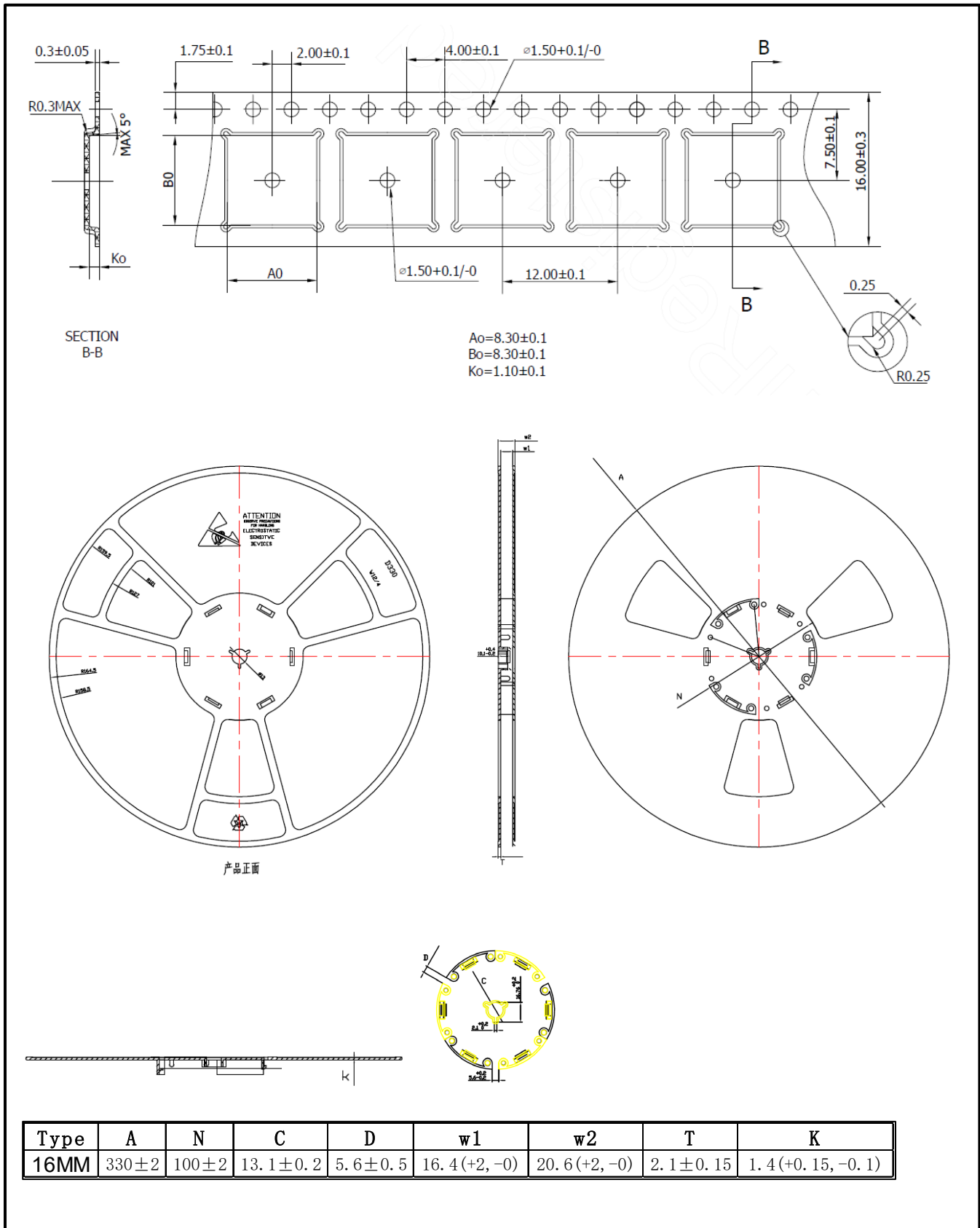
10. Package outlines



Notes:

- (1) Dimension and tolerance conform to ASME Y14.5-2009.
- (2) All dimension are in millimeters.
- (3) Lead coplanarity shall be 0.1 millimeters max.
- (4) Complies with JEDEC MO-229.
- (5) Drawing is not to scale.

11. Reel Information



12. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2021-4-23	1.0 version release

Important Notice

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