JWH6346

High Efficiency
Synchronous Step-Down PWM Controller

DESCRIPTION

The JW®H6346 is a synchronous buck regulator controller. Operating with an input range of 6V~75V, the JWH6346 adopts voltage mode control and provides high efficiency, excellent transient response, and high DC output accuracy needed for low output voltage, high current, PC system power rail and similar POL power supply in digital consumer products.

The JWH6346 guarantees robustness with thermal protection, short-circuit protection, over current protection and VCC under voltage protection.

The JWH6346 is available in QFN3.5X4.5-20 package, which provides a compact solution with minimal external components.

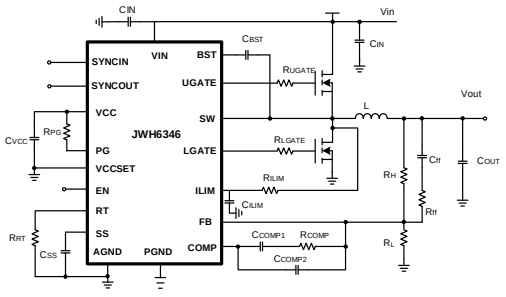
FEATURES

- 6V to 75V operating input range without external VCC
- 5V to 100V operating input range with external VCC
- 0.8V to 60V output voltage range
- Built-in ±1% 0.8V reference voltage
- Switching frequency from 100kHz to 1MHz
  -SYNC in and SYNC out capability
- 7.5V or 10V gate drivers for standard V_{TH} MOSFETs
  -25ns dead time
  -2.3A source and 3.5A sink capability
  -Low-side soft-start for pre-bias start-up
- Programmable current limit by low side $R_{DS(ON)}$ sensing or shunt sensing
- Adjustable soft-start or optional voltage tracking
- Built-in OCP/UVP
- Power good indicator
- Thermal protection
- Available in QFN3.5X4.5-20 package

APPLICATIONS

- Networking and Computing Power
- Industrial Motor Drive

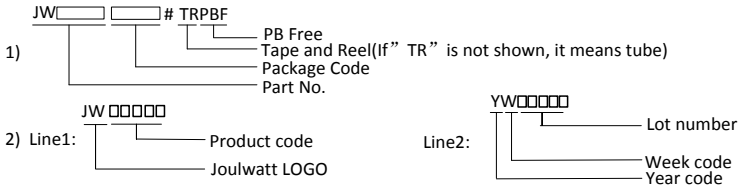
TYPICAL APPLICATION



ORDER INFORMATION

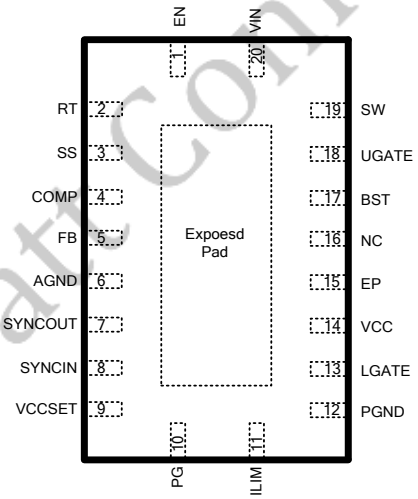
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JWH6346QFNAC#TRPBF	QFN3.5X4.5-20	JWH6346 YW□□□□□

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN Pins ..... -0.3V to 105V
SW Pin ..... -1V(-10V for 20ns) to 105V
BST Pin ..... SW-0.3V to SW+14V
ILIM Pin ..... -0.6V to 105V
VCC, PG, SYNCIN, VCCSET Pins ..... -0.3V to 14V
FB, COMP, SS, RT Pins ..... -0.3V to 6V
UGATE to SW Pin ..... -0.3V (-10V for 20ns) to 14V
LGATE to GND Pin ..... -0.3V(-10V for 20ns) to 14V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC
ESD Susceptibility (Human Body Model)..... 2kV
ESD Susceptibility (Charged Device Model).....500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN without External VCC .....6V to 75V
Input Voltage VIN with External VCC .....5V to 100V
External VCC .....8V to 13V
Output Voltage Vout.....0.8V to 60V
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}	θ_{Jb}
QFN3.5X4.5-20	37	2.1	11.8 ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH6346 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{EN}=1.5V, R_{RT}=25kΩ, T_J = -40ºC~125ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Shutdown Current	I_{SD}	V_{EN}=0V, V_{VCC}<1V，TA=25℃		15	20	μA
Standby Input Current	I_{Q_STBY}	V_{EN}=1V		450	800	uA
Operating Input Current, Not Switching	I_{Q_RUN}	V_{EN}=1.5V, V_{SS}=0V		600	800	uA
V_{CC} Under-voltage Lockout Threshold	V_{VCC_MIN}	V_{VCC} rising	4.8	5	5.2	V
V_{CC} Under-voltage Lockout Hysteresis	$V_{VCC\_MIN\_HYST}$	V_{VCC} falling		370		mV
V_{CC} Regulation Voltage	V_{VCC}	V_{SS}=0V, 9V≤V_{IN}≤75V, 0mA≤I_{VCC}≤20mA, V_{VGSET}=GND or floating	7.3	7.5	7.7	V
		V_{SS}=0V, 12V≤V_{IN}≤75V, 0mA≤I_{VCC}≤20mA, V_{VGSET}≥5V	9.7	10	10.3	V
VIN to VCC dropout voltage	V_{VCC_LDO}	V_{IN}=6V, V_{SS}=0V , I_{VCC}=20mA		0.4	0.7	V
VCC Short-circuit Current Limit	I_{SC_LDO}	V_{SS}=0V , V_{VCC}=0V,	40	60	90	mA
Minimum External Bias Supply Voltage	V_{VCC_EXT}	Voltage required to disable VCC regulator, V_{VGSET}=GND or floating	8			V
External VCC Input Current, Not Switching	I_{VCC}	V_{SS}=0V , V_{VCC}=13V,			2.1	mA
Feedback Voltage	V_{FB}	FB connected to COMP	792	800	808	mV
FB Input Bias Current	I_{FB}	V_{FB}=0.8V	-0.1		0.1	μA
COMP Output High Voltage[5)]	V_{COMP_HO}	V_{FB}=0V, COMP souring 1mA		5		V
COMP Output Low Voltage	V_{COMP_LO}	COMP sinking 1mA		0.5		V
Error Amplifier DC Gain[5)]	Gain			110		dB
Enable Shutdown to Standby Threshold	V_{SDN}	V_{EN} rising		0.4		V
Enable Shutdown Threshold	V_{SDN_HYS}	V_{EN} falling		50		mV
Enable Standby to Operating Threshold	V_{EN}	V_{EN} rising	1.164	1.2	1.236	V

Enable Standby to Operating Threshold	V_{EN_L}	V_{EN} falling	1	1.09	1.18	V
Enable Standby to Operating Threshold Hysteresis	V_{EN_HYS}	V_{EN} falling		115		mV
Enable Standby to Operating Hysteresis Current		V_{EN} =1.5V	9	10	11	μA
Minimum Controllable On Time[5]	T_{ON_MIN}	V_{BST}-V_{SW}=7V, UGATE 50% to 50%		40	60	ns
Minimum Off Time[5]	T_{OFF_MIN}	V_{BST}-V_{SW}=7V, UGATE 50% to 50%		210	320	ns
Maximum Duty cycle	D_{MAX}	Fsw=100kHz, 6V≤V_{IN}≤60V	95%	97%		
		Fsw=400kHz, 6V≤V_{IN}≤60V	86%	89%		
Ramp valley voltage (COMP at 0% duty cycle)	V_{RAMP_MIN}			500		mV
PWM Feed-forward Gain[5]	k_{FF}	6V≤V_{IN}≤100V,		15		V/V
Internal Boot Strap Switch On resistance	R_{BST}				9	Ω
BST to SW Quiescent Current, Not Switching	I_{Q_BST}	V_{SS}=0V, V_{BST}=54V, V_{SW}=48V		45		μA
BST to SW Under-voltage Detection	V_{BST_UV}	V_{BST}-V_{SW} Falling		3.6		V
BST to SW Under-voltage Hysteresis	V_{BST_HYS}	V_{BST}-V_{SW} Rising		0.4		V
ILIM Source Current	I_{RS}	R_{SENSE} Mode	90	100	110	μA
	I_{RDSON}	R_{DSON} Mode@25℃	180	200	240	μA
ILIM Source Current TC[5]	I_{RSTC}	R_{SENSE} Mode		0		ppm/ ºC
	$I_{RDSONTC}$	R_{DSON} Mode		4500		ppm/ ºC
ILIM comparator threshold at ILIM[5]	V_{ILIM_TH}		-8	-2	3.5	mV
SCP Clamp Offset Voltage[5]	V_{CLAMP_OS}	Clamp to COMP steady state offset voltage	0.56+ V_{IN}/75			V
Minimum Clamp Voltage[5]	V_{CLAMP_MIN}	Clamp voltage with continuous current limiting	0.56+V_{IN}/150			V
Hiccup Mode Activation Delay[5]	C_{HICC_DEL}			128		cycles
Hiccup Mode Off-time After Activation[5]	C_{HICCUP}			8192		cycles
Zero-cross Detect Disable Threshold (CCM)[5]	V_{ZCD_DIS}			200		mV
Zero-cross Detect Soft-start	V_{ZCD_SS}			0		mV

Ramp[5)]						
Diode Emulation Zero-cross Threshold[5)]	$V_{DE,\_TH}$	Measured at SW with V_{SW} rising	-5	0	5	mV
SS Charge Current	I_{SS}	V_{SS}=0V	8.5	10	12	μA
SS Discharge FET Resistance	R_{SS_DIS}	V_{EN}= 0.8V, V_{SS}=0.1V		11		Ω
SS to FB Offset	V_{SS_FB}		-15		15	mV
SS Clamp Voltage	V_{SS_CLAMP}	V_{SS} - V_{FB}, V_{FB} = 0V		0.1		V
UGATE Drive Source	R_{UGATE_SR}	V_{BST}-V_{SW}=7V, I_{UGATE}=-100mA		1.5		Ω
UGATE Drive Sink	R_{UGATE_SK}	V_{BST}-V_{SW}=7V, I_{UGATE}=100mA		0.9		Ω
LGATE Drive Source	R_{LGATE_SR}	V_{VCC}=7V, I_{LGATE}=-100mA		1.5		Ω
LGATE Drive Sink	R_{LGATE_SK}	V_{VCC}=7V, I_{LGATE}=100mA		0.9		Ω
UGATE, LGATE Source Current[5)]	I_{UGATEH}, I_{LGATEH}	V_{BST} – V_{SW} = 7 V, UGATE = SW, LGATE = AGND		2.3		A
UGATE, LGATE Sink Current[5)]	I_{UGATEL}, I_{LGATEL}	V_{BST} – V_{SW} = 7 V, UGATE = BST, LGATE = VCC		3.5		A
Dead Time[5)]	T_D	V_{BST}-V_{SW}=7V, LGATE off to UGATE on, 50% to 50%		25		ns
		V_{BST}-V_{SW}=7V, UGATE off to LGATE on, 50% to 50%		25		ns
UGATE, LGATE Rising Times[5)]	T_{TR}	V_{BST}-V_{SW}=7V, C_{LOAD}=1nF, 20% to 80%		7		ns
UGATE, LGATE Falling Times[5)]	T_{TF}	V_{BST}-V_{SW}=7V, C_{LOAD}=1nF, 80% to 20%		4		ns
Power Good Lower Threshold	PG_{LTH}	% of V_{REF} , FB falling, hysteresis=2%	89.7%	92.7%	95.7%	
Power Good Upper Threshold	PG_{UTH}	% of V_{REF} , FB rising, hysteresis=3%	105%	108%	111%	
Power Good Delay	PG_{DLY}	PG from low to high or low to high		36		us
Power Good Sink Current	I_{PG}	V_{FB}=0.9V, V_{PG}=0.4V	4			mA
Oscillator Frequency	F_{SW}	R_{RT}=100k	80	100	120	kHz
		R_{RT}=25k	370	400	430	kHz
		R_{RT}=12.5k	675	740	805	kHz
SYNCIN External Clock Frequency Range	F_{SYNC}	% of nominal frequency set by R_{RT}	-30%		50%	
Minimum SYNCIN Input Logic High	V_{SYNC_IH}		3			V
Minimum SYNCIN Input Logic	V_{SYNC_IL}				0.5	V

Low						
SYNCIN Input Resistance	R_{SYNCIN}	V_{SYNCIN}=3V		17.5		kΩ
SYNCIN Input Minimum Pulse Width	T_{SYNCIN_PW}	Minimum high state	50			ns
SYNCOUT High-state Output Voltage	$V_{SYNCOUT\_H}$	$I_{SYNCOUT}$=-1mA (souring)	3			V
SYNCOUT Low-state Output Voltage	$V_{SYNCOUT\_L}$	$I_{SYNCOUT}$=1mA (sinking)			0.4	V
Delay from UGATE Rising to SYNCOUT Leading Edge	$T_{SYNCOUT}$	V_{SYNCIN}=0V, T_S=1/F_{SW}, F_{SW} set by R_{RT}	T_S/2-220			ns
Delay from SYNCIN Leading Edge to UGATE Rising	T_{SYNCIN}	50% to 50%		250		ns
VCCSET Logic High Input Voltage	V_{VCCSET_H}		5			V
VCCSET Logic Low Input Voltage	V_{VCCSET_L}				0.7	V
Thermal Shutdown[5)]	T_{TSD}	T_J rising		180		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYS}			20		°C

Note：

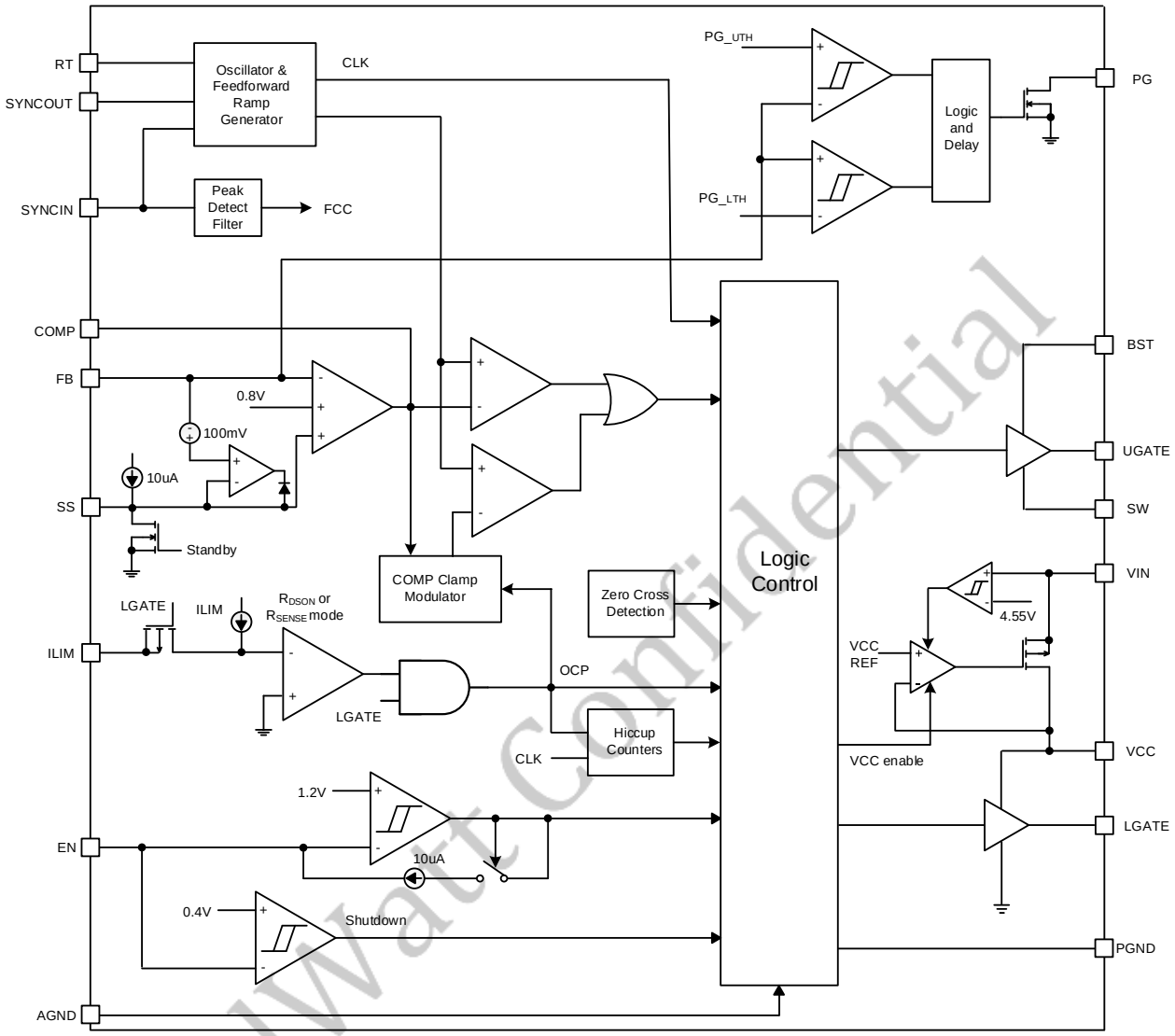
5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	EN	Enable input pin. If the EN voltage is lower than 0.4V, the device entry shutdown mode with all function disabled; if the EN voltage is higher than 0.4V and lower than 1.2V, the regulator is in standby mode which the VCC regulator operational, the SS pin grounded and no switching at the UGATE/LGATE outputs; if the EN voltage is higher than 1.2V, the device entry normal operation mode. Once the EN voltage rises above the 1.2V threshold, a 10uA current source is enabled and flows through the external UVLO resistor divider to generate a hysteresis. The hysteresis at EN pin can be adjusted by the resistance of the external divider.
2	RT	Oscillator frequency program input. Connect a resistor from this pin to AGND to program the internal oscillator frequency. An RT resistor is required even when using the SYNCIN pin to synchronize to an external clock.
3	SS	External soft-start pin. A minimum capacitance from SS to AGND of 2.2nF is required.
4	COMP	Low impedance output if the internal error amplifier. The loop compensation network should be connected between COMP pin and FB pin.
5	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 800mV. Connect a resistive divider at FB pin.
6	AGND	Analog ground.
7	SYNCOUT	Synchronization output.
8	SYNCIN	Dual function pin for providing an optional clock input and for enabling diode emulation by the low-side MOSFET. Connecting a clock signal to the SYNCIN pin synchronizes switching to the external clock. Diode emulation by the low-side MOSFET is disabled when the controller is synchronized to an external clock, and negative inductor current can flow in the low-side MOSFET with light loads. A continuous logic low state at the SYNCIN pin or leave SYNCIN pin floating enables diode emulation to prevent reverse current flow in the inductor. Diode emulation results in DCM operation at light loads, which improves efficiency. A logic high state at the SYNCIN pin disables diode emulation producing forced-PWM (FCC) operation.
9	VCCSET	VCC regulation voltage setting pin. Pull the VCCSET pin higher than 5V, the VCC regulation voltage is 10V; Pull the VCCSET pin to ground or leave this pin floating, the VCC regulation voltage is 7.5V.
10	PG	Open drain output for power-good indicator. Use a10kΩ to 100kΩ pull-up resistor to logic rail or other DC voltage no higher than 13V.
11	ILIM	Current limit adjust and current sense comparator input. An external resistor connected to the ILIM pin is used to program the valley current limit and the opposite end of the resistor can be connected to either the drain of the low-side MOSFET for RDS(on) sensing or to a current sense resistor connected to the source of the low-side FET.
12	PGND	Power ground.
13	LGATE	Gate drive output for low side external MOSFET. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.

14	VCC	Output of the internal regulator output. Bypass to GND with a minimum 1uF ceramic capacitor.
15	EP	Pin internally connected to exposed pad of the package.
16	NC	No connection.
17	BST	Bootstrap pin for top switch. Connect through a capacitor to SW pin.
18	UGATE	Gate drive output for high side external MOSFET. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.
19	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
20	VIN	Supply voltage for the internal VCC regulator.
Exposed-pad		Exposed pad of the package. The exposed pad is recommended to be soldered to a large PCB and connected to GND for maximum power dissipation.

BLOCK DIAGRAM



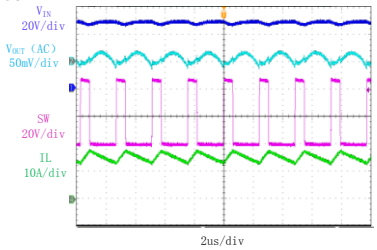
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=48V, V_{OUT}= 12V, L = 4.5μH, C_{OUT} = 47*5μF, R_T = 24.9KΩ, T_A = +25°C, unless otherwise noted

Steady State Test

V_{IN}=48V, V_{OUT}=12V

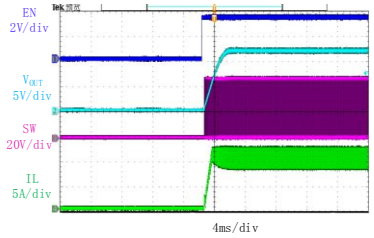
I_{OUT}=15A



Startup through Enable

V_{IN}=48V, V_{OUT}=12V

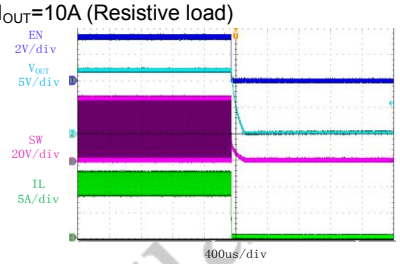
I_{OUT}=10A (Resistive load)



Shutdown through Enable

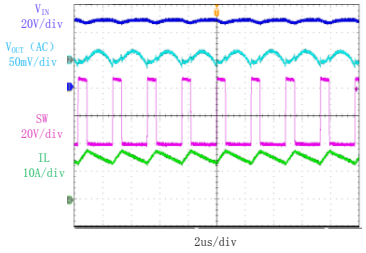
V_{IN}=48V, V_{OUT}=12V

I_{OUT}=10A (Resistive load)



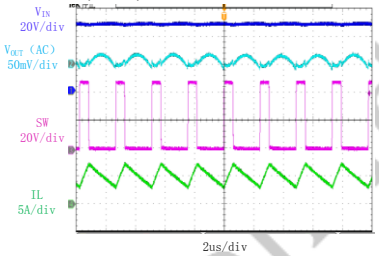
Heavy Load Operation

15A LOAD(PFM)



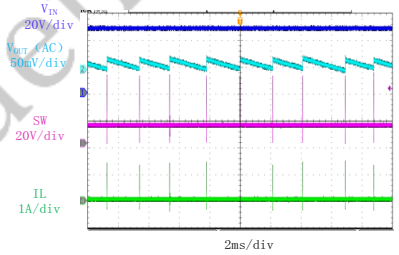
Light Load Operation

5A LOAD(PFM)



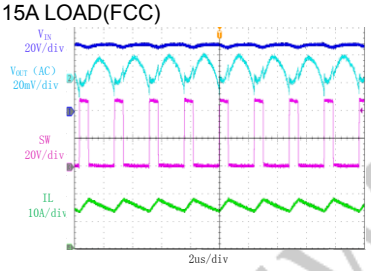
No Load Operation

0 A LOAD(PFM)



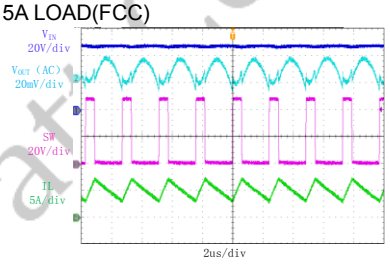
Heavy Load Operation

15A LOAD(FCC)



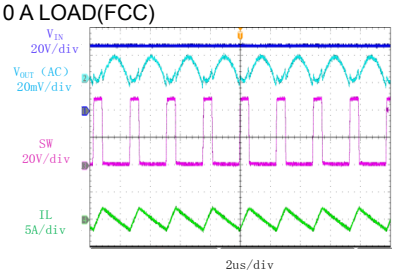
Light Load Operation

5A LOAD(FCC)



No Load Operation

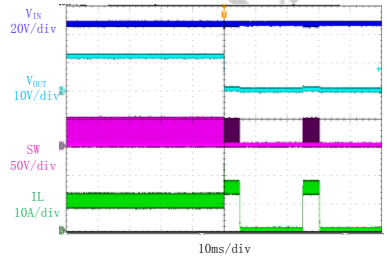
0 A LOAD(FCC)



Short Circuit Protection

V_{IN}=48V, V_{OUT}=12V

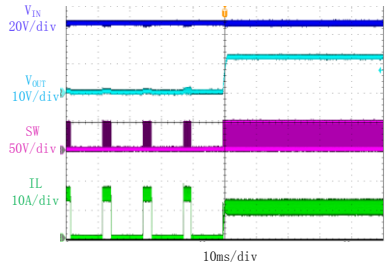
I_{OUT}=10A- Short



Short Circuit Recovery

V_{IN}=48V, V_{OUT}=12V

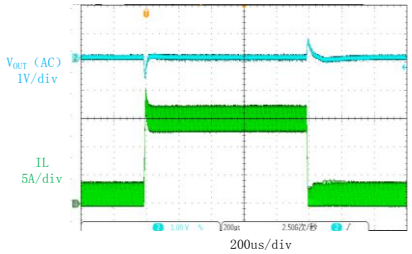
I_{OUT}= Short-10A



Load Transient

1.5A LOAD → 15A LOAD →1.5A LOAD

Rate=2.5A/us



TYPICAL PERFORMANCE CHARACTERISTICS

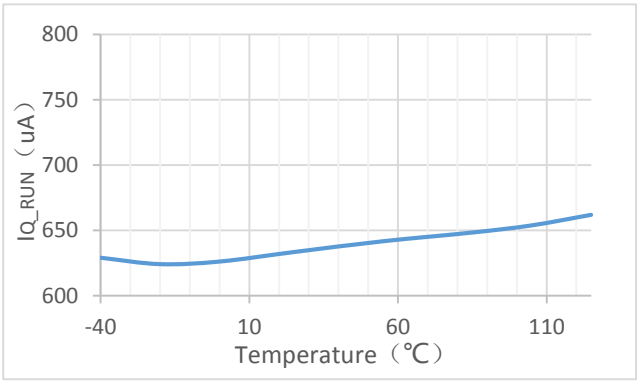


Figure 1. Operating Input Current vs Junction Temperature

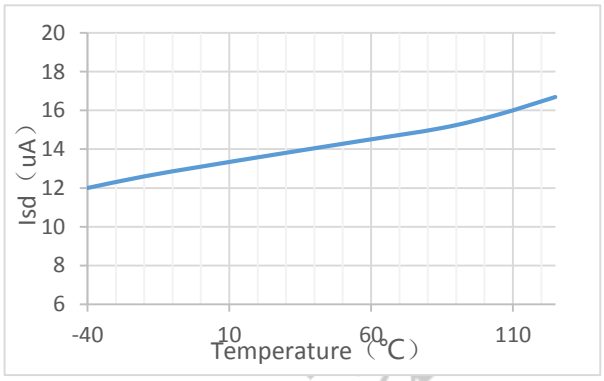


Figure 2. Shutdown Current vs Junction Temperature

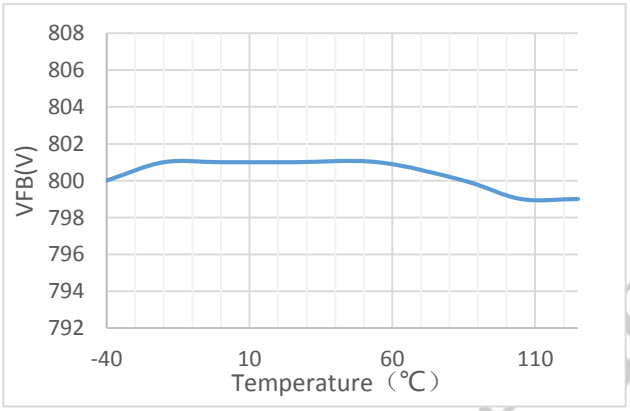


Figure 3. FB Voltage Regulaion vs Junction Temperature

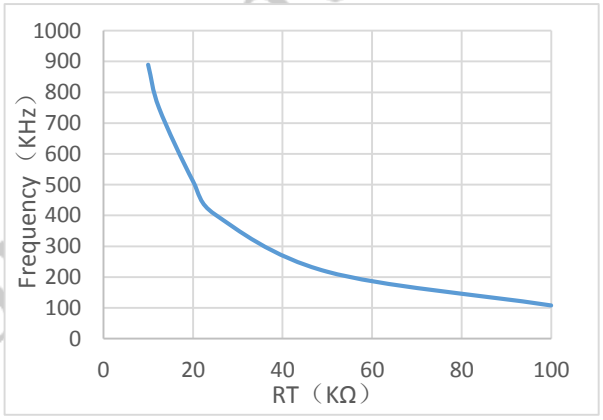


Figure 4. Switch Frequency vs RT

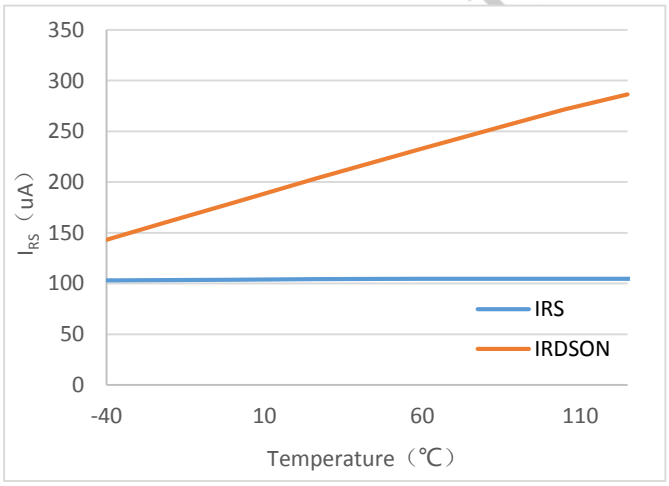


Figure 5. ILIM Current Source vs Junction Temperature

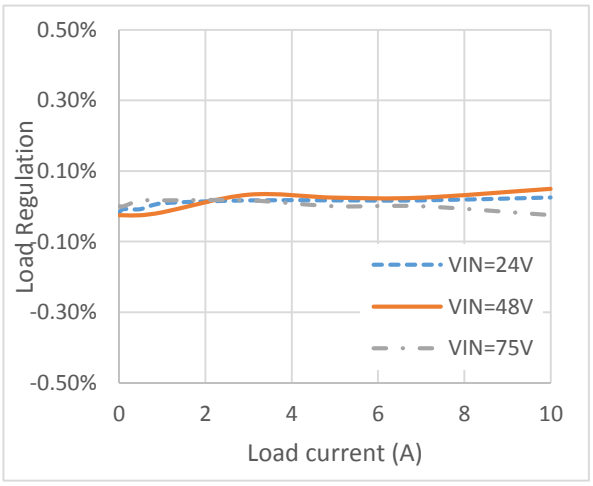


Figure 6. Load Regulation

(Vout=12V, L=4.5μH,Frequency=400kHz,FCC)

TYPICAL PERFORMANCE CHARACTERISTICS

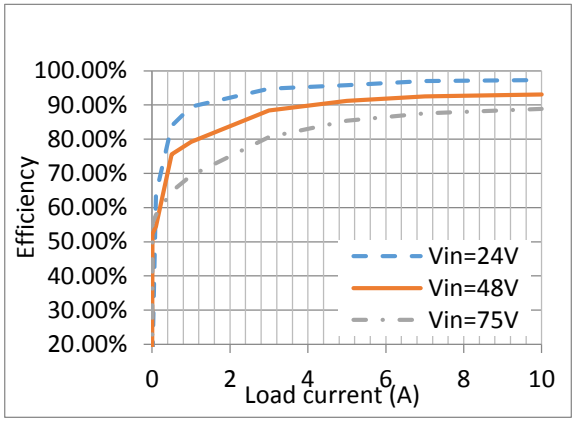


Figure 7. Efficiency vs Load Current

(Vout=12V, L=4.5μH,Frequency=400kHz,PFM)

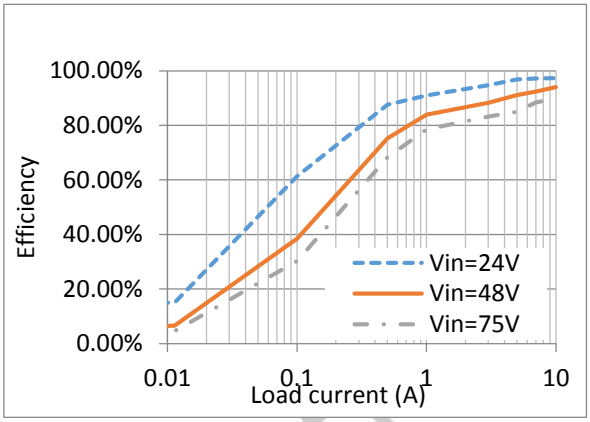


Figure 8. Efficiency vs Load Current

(Vout=12V, L=4.5μH,Frequency=400kHz,FCC)

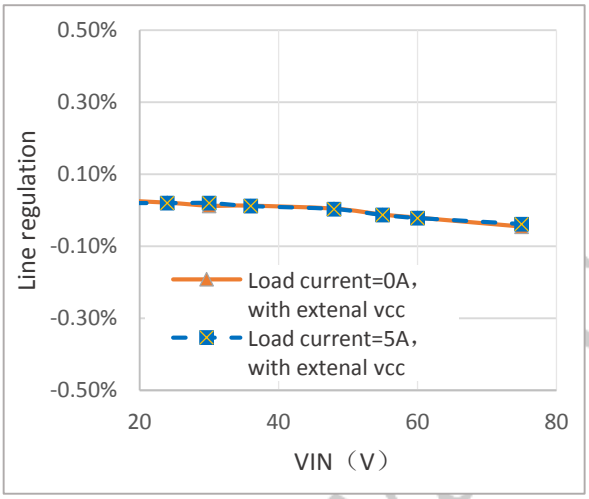


Figure 9. Line Regulation

(Vout=12V, L=4.5μH,Frequency=400kHz,FCC)

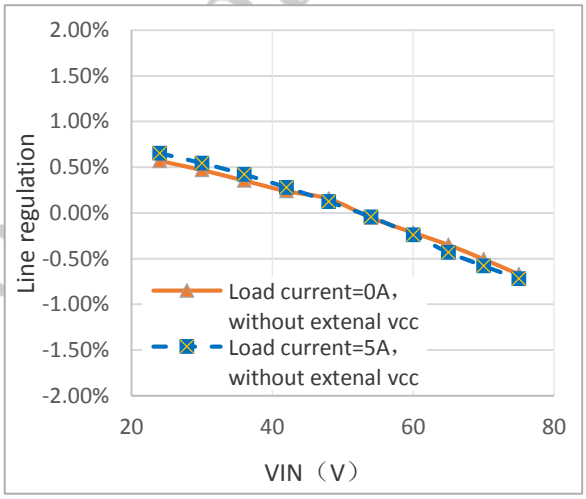


Figure 10. Line Regulation

(Vout=12V, L=4.5μH,Frequency=400kHz,FCC)

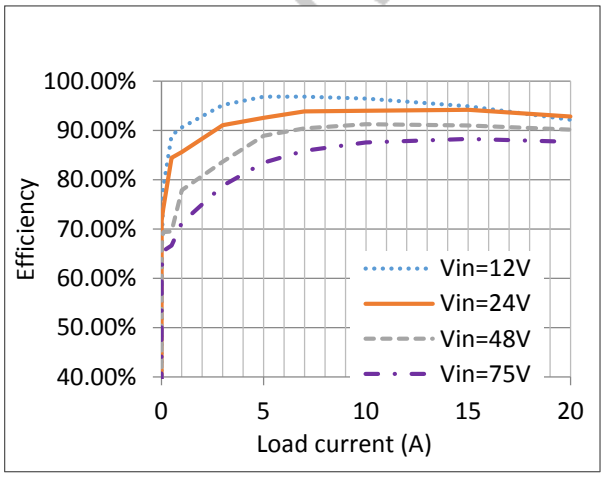


Figure 11. Efficiency vs Load Current

(Vout=5V, L=3.5μH,Frequency=200kHz,PFM)

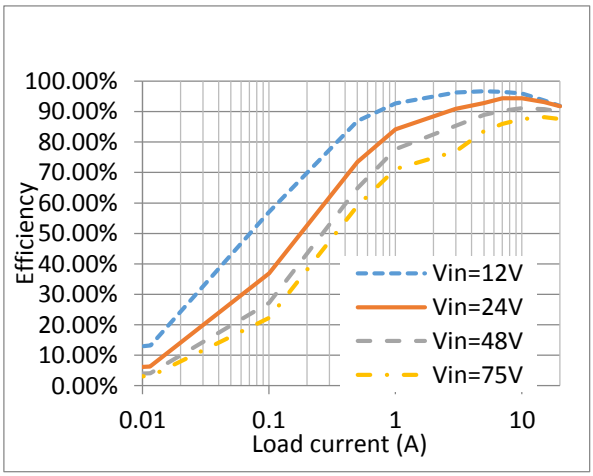


Figure 12. Efficiency vs Load Current

(Vout=5V, L=3.5μH,Frequency=200kHz,FCC)

FUNCTIONAL DESCRIPTION

The JWH6346 is a synchronous step-down PWM controller. It adopts voltage mode control and regulates input voltages from 6V to 75V down to an output voltage as low as 0.8V. The input voltages can be from 5V to 100V with external VCC.

Voltage-Mode Control

The JWH6346 utilizes a voltage-mode control with input voltage feed-forward to eliminate the input voltage dependence of the PWM modulator. A ramp is generated internally for the PWM modulation and the ramp voltage amplitude increases with input voltage increases to maintain constant modulator gain. The ramp is initialed at the falling edge of the internal clock and the high-side MOSFET is turned on at the same time. The output voltage is measured at the FB pin through a resistive voltage divider. The FB voltage is compared to the internal 0.8V reference voltage and the error is amplified by internal trans conductance error amplifier. The output of the error amplifier (COMP) is compared with the ramp and once the ramp voltage rises above the COMP voltage, the high-side MOSFET is turned-off and the low-side MOSFET turns on until the falling edge of the clock comes.

PFM Mode

With SYNCIN pin pulled down to low or leave SYNCIN pin floating, the JWH6346 operates in PFM mode at light load. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

FCC Mode

When the SYNCIN pin is tied high, the controller keeps continuous conduction mode in light load condition. In this mode, switch frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

Shut-Down Mode

The JWH6346 shuts down when voltage at EN pin is below 0.4V. The entire controller is off and the supply current consumed by the JWH6346 drops below 15uA.

Standby Mode

When voltage at EN pin rises above 0.4V and is below the precision enable threshold 1.2V(typ.), the JWH6346 enters standby mode. In the standby mode, the internal bias supply LDO is on and regulating but the switching action and output voltage regulation are disabled.

Active Mode

When voltage at EN pin rises above the precision enable threshold 1.2V(typ.) and the VCC voltage is above its rising UVLO threshold of 5V, the JWH6346 enters active mode. In active mode, all the functions are enabled.

Precision Enable and Adjustable UVLO Protection

The JWH6346 support adjustable input under-voltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements and a resistive divider connected between V_{IN} and ground with the central tap

connected to EN can be used to adjust the input voltage UVLO. (Shown in Figure13). Once the EN pin voltage exceeds 1.2 V, an additional 10μA of hysteresis is added. This hysteresis current and the hysteresis voltage of the EN comparator itself will contribute to the hysteresis of the input voltage. Use below equation to set the input startup voltage and external hysteresis for the input voltage.

$$R_{EN\_H} = \frac{(V_{EN} - V_{HYS})V_{STR} - V_{EN} \times V_{STOP}}{V_{EN} \times I_{HYS}}$$

$$R_{EN\_L} = R_{EN\_H} \times \frac{V_{EN}}{V_{STR} - V_{EN}}$$

If the hysteresis voltage of the EN comparator itself is not considered, the following formula can be used for rough calculation:

$$R_{EN\_H} = \frac{V_{STR} - V_{STOP}}{I_{HYS}}$$

$$R_{EN\_L} = R_{EN\_H} \times \frac{V_{EN}}{V_{STR} - V_{EN}}$$

where I_{HYS}=10uA, V_{EN} =1.2V, V_{HYS}=115mV.

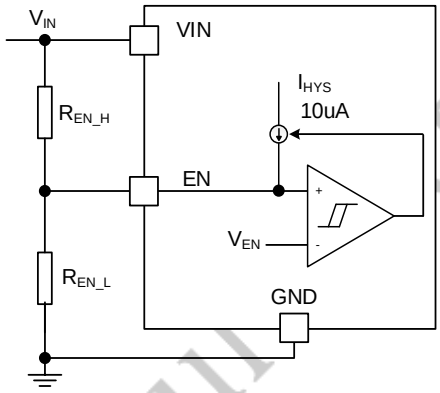


Figure13. UVLO Setting

VCC Regulator

JWH6346 has an internal high-voltage VCC regulator that provides the power supply for the PWM controller and its gate driver for the external MOSFETs. The output of the VCC regulator can be set by the VCCSET pin. If the VCCSET pin pulled low or floating, the output of the VCC regulator is 7.5V in typical; and if the VCCSET pin pulled high, the output of VCC regulator is 10V in typical. When the input voltage drops below the VCC set-point level, the VCC output tracks VIN with a small voltage drop. Connect a ceramic decoupling capacitor between 1 μF and 5 μF from VCC to AGND for stability.

The VCC regulator has a current limit of 40mA (minimum) and under-voltage lockout protection. When the VCC voltage exceeds its rising UVLO threshold of 5 V, the output is enabled (if EN/UVLO is above 1.2 V) and the soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of 4.63V (typical) or if EN/UVLO goes to a standby or shutdown state.

Internal power dissipation of the VCC regulator can be minimized by connecting the output voltage or an auxiliary bias supply rail (up to 13 V) to VCC using a diode D_{VCC}. This method can reduce the influence of internal VCC regulator circuit heating on the reference voltage. A diode in series with the input prevents reverse current flow from VCC to V_{IN} if the input voltage falls below the external VCC rail.

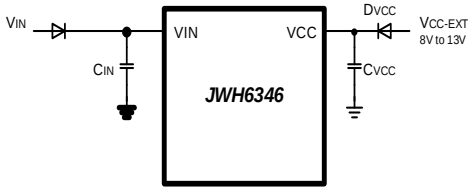


Figure14. VCC Bias Supply Connection from V_{OUT} or Auxiliary Supply

MOSFET Gate Driver

The high-side driver is designed to drive high current, low R_{DSON} N-MOSFET(s). When configured as a floating driver, 7.5V (or 10V) of bias voltage is delivered from VCC supply. The average drive current is also equal to the gate charge at V_{GS}=7.5V (or 10V) times switching frequency. The instantaneous drive current is supplied by the bootstrap capacitor between BST and SW pins. The drive capability is represented by its internal resistance, which are 1.5Ω for BST to UGATE and 0.9Ω for UGATE to

SW.

The low-side driver is designed to drive high current, low R_{DSON} N-MOSFET(s). The drive capability is represented by its internal resistance, which are 1.5Ω for VCC to LGATE and 0.9Ω for LGATE to GND. 7.5V (or 10V) bias voltage is delivered from VCC supply. The instantaneous drive current is supplied by an input capacitor connected between VCC and GND. The average drive current is equal to the gate charge at V_{GS}=7.5V (or 10V) times switching frequency. This gate drive current as well as the high-side gate drive current times 7.5V (or 10V) makes the driving power which need to be dissipated from JWH6346 package. An adaptive dead time is designed to present shoot through between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

External Soft-start

Soft-start is designed in JWH6346 to prevent the converter output voltage from overshooting during startup and short-circuit recovery and the soft-start time can be adjusted by a capacitor connected between SS pin and AGND. When the chip starts, a 10uA current source charges the SS capacitor and the soft-start time can be calculated by below Equation.

$$t_{ss} = \frac{C_{SS} * V_{REF}}{I_{SS}}$$

where C_{SS} is the SS capacitance between SS pin and AGND;

V_{REF} is the 0.8V internal reference voltage;

I_{SS} is the 10uA current sourced from SS pin.

When an overload event or short circuit event happens, the SS pin is internally clamped to V_{FB} +100mV to allow a soft-start recovery and the clamp circuit requires a soft-start capacitance greater than 2nF for stability.

Current Sense and Over-Current Protection

JWH6346 has a cycle-by-cycle overcurrent limiting control. A valley current limit is designed in the JWH6346 so that only when output current drops below the valley current limit can the high-side MOSFET be turned on. To provide both good accuracy and cost effective solution, the JWH6346 supports temperature compensated MOSFET R_{DSON} sensing mode and shunt resistor sensing mode, and it detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly. Figure15 portrays the R_{DSON} sensing mode which resistor R_{ILIM} is tied to SW to use the R_{DSON} of the low-side MOSFET as a sensing element (termed R_{DSON} mode) and Figure16 shows the shunt resistor sensing mode which R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET (termed R_{SENSE} mode).

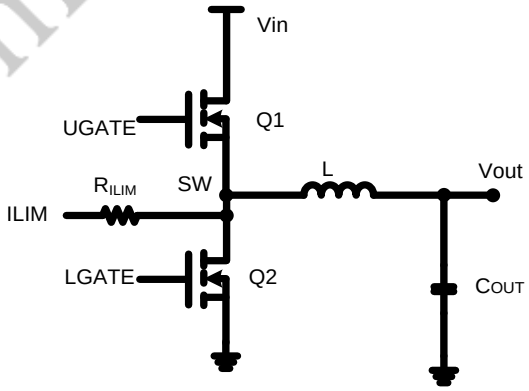


Figure15. MOSFET R_{DSON} Current Sensing

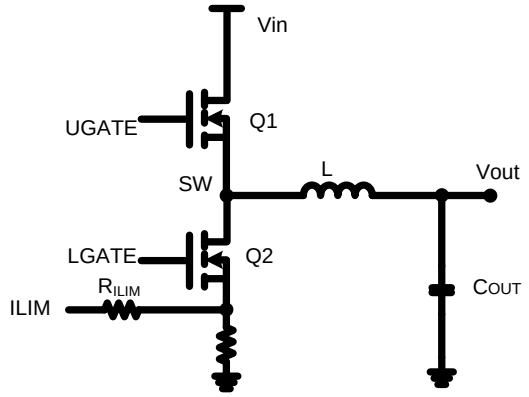


Figure16. Shunt Resistor Current Sensing

The ILIM pin of the JWH6346 sources a reference current that flows in an external resistor, designated R_{ILIM}, to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND.

The ILIM current with R_{DSON} sensing is 200 μA at 25°C junction temperature and incorporates a TC of +4500 ppm/°C to generally track the R_{DSON} temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100 μA in R_{SENSE} mode. This controls the valley of the inductor current during a steady state overload at the output. Depending on the chosen mode, select the resistance of R_{ILIM} using below equation.

$$R_{ILIM} = \frac{I_{OUT} - \Delta I_L/2}{I_{RDSON}} * R_{DSON} \quad (R_{DSON} \text{ mode})$$

$$R_{ILIM} = \frac{I_{OUT} - \Delta I_L/2}{I_{RS}} * R_S \quad (R_{SENSE} \text{ mode})$$

where

R_{DSON} is the on-resistance of low-side MOSFET;

ΔI_L is the peak-to peak inductor ripple current;

I_{RDSON} is the ILIM pin current in R_{DSON} mode;

R_S is the resistance of current sensing shunt element; I_{RS} is the ILIM pin current in R_{SENSE} mode.

In addition to valley current limiting, the JWH6346 uses a proprietary duty-cycle limiter circuit to reduce the PWM on-time during an overcurrent condition. As shown in Figure17, an auxiliary PWM comparator along with a modulated CLAMP voltage limits how quickly the on-time increases in response to a large step in the COMP voltage that typically occurs with a voltage-mode control loop architecture. As depicted in Figure17, the CLAMP voltage, VCLAMP, is normally regulated above the COMP voltage to provide adequate headroom during a response to a load-on transient. If the COMP voltage rises quickly during an overloaded or shorted output condition, the on-time pulse terminates thereby limiting the on-time and peak inductor current. Moreover, the CLAMP voltage is reduced if additional valley current limit events occur, further reducing the average output current.

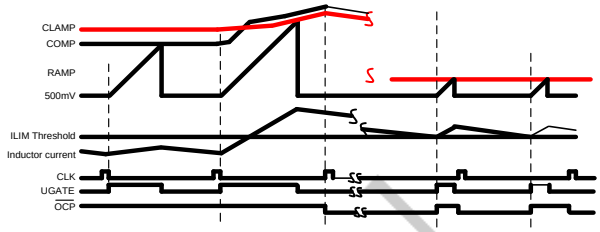


Figure17. OCP Duty Cycle Limiting Waveforms

If the overcurrent condition exists for 128 continuous clock cycles, a hiccup event is triggered and SS is pulled low for 8192 clock cycles before a soft-start sequence is initiated.

Power Good

The JWH6346 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to a voltage source (such as V_{OUT}) through a resistor (10kΩ to 100kΩ). When the FB voltage exceeds 94% of the internal reference V_{REF}, internal comparators detect power good state and the power good signal becomes high with 36us deglitch delay time. If the feedback voltage goes under 92% of the target value, the power good signal becomes low with 36us deglitch delay time. Similarly, when the FB voltage exceeds 108% of the internal reference V_{REF}, the power good signal becomes low with 36us deglitch delay time. If the FB voltage subsequently falls below 105% of V_{REF}, the power good signal becomes high.

Switching Frequency

The switching frequency can be adjusted by the resistor connected between RT pin and AGND, or synchronizing the JWH6346 to an external clock signal through the SYNCIN pin.

The switching frequency range adjusted by the

RT resistor is from 100 kHz to 1MHz, and the RT resistance can calculate by the Equation 5.

$$R_{RT}(k\Omega) = \frac{10^4}{f_{sw}(kHz)} - 0.3$$

Clock Synchronization

The switching frequency in CCM state of JWH6346 can be synchronized to an external clock and the requirements for the external clock SNYC signal are:

Clock range: 100kHz to 1MHz

Clock frequency range: -30% to +50% of the free-running frequency set by RRT

Clock maximum voltage amplitude: 13V

Clock minimum pulse width: 50ns

Thermal Protection

When the junction temperature of the JWH6346 rises above 175°C, it is forced into thermal shut-down which both the high-side and low-side MOSFETs are turned off and the SS and PG are pulled low.

Only when the junction temperature drops below 155°C can the device restart again.

APPLICATION INFORMATION

Output Voltage Set

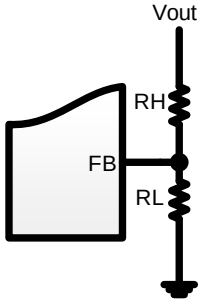
The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{out} * \frac{R_L}{R_H + R_L}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

If R_L is determined, and then R_H can be calculated by:

$$R_H = R_L * \left(\frac{V_{out}}{0.8} - 1\right)$$



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{out}}{V_{in}} * \left(1 - \frac{V_{out}}{V_{in}}\right)}$$

where I_{OUT} is the load current, V_{out} is the output voltage, V_{in} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_{SW} * \Delta V_{in}} * \frac{V_{out}}{V_{in}} * \left(1 - \frac{V_{out}}{V_{in}}\right)$$

where C_{IN} is the input capacitance value, f_{sw} is the switching frequency, ΔV_{in} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 4.7μF*2/100V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{out} = \frac{V_{out}}{f_{SW} * L} * \left(1 - \frac{V_{out}}{V_{in}}\right) * \left(R_{ESR} + \frac{1}{8 * f_{SW} * C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage. The output capacitors also affect the system stability and transient response.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{out}}{f_{SW} * \Delta I_L} * \left(1 - \frac{V_{out}}{V_{in}}\right)$$

where V_{in} is the input voltage, V_{out} is the output voltage, f_{sw} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

$$I_{Lpeak} = I_{out} + 0.5 * \Delta I_L$$

Check the inductor datasheet to ensure that the saturation current of the inductor is well above the peak inductor current of a particular design.

External Bootstrap Capacitor

The bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1μF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

Power MOSFETs

The choice of power MOSFETs has significant impact on DC-DC regulator performance. A MOSFET with low on state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS} respectively),. As a result, the product $R_{DS(on)} \times Q_G$ is commonly specified as a MOSFET figure-of-merit. Low thermal resistance ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in anJWH6346 application are as follows:

• $R_{DS(on)}$ at V_{GS} = 7.5 V;

• Drain-source voltage rating, BV_{DSS}, typically 60 V, 80 V or 100 V, depending on maximum input voltage;

• Gate charge parameters at V_{GS} = 7.5 V;

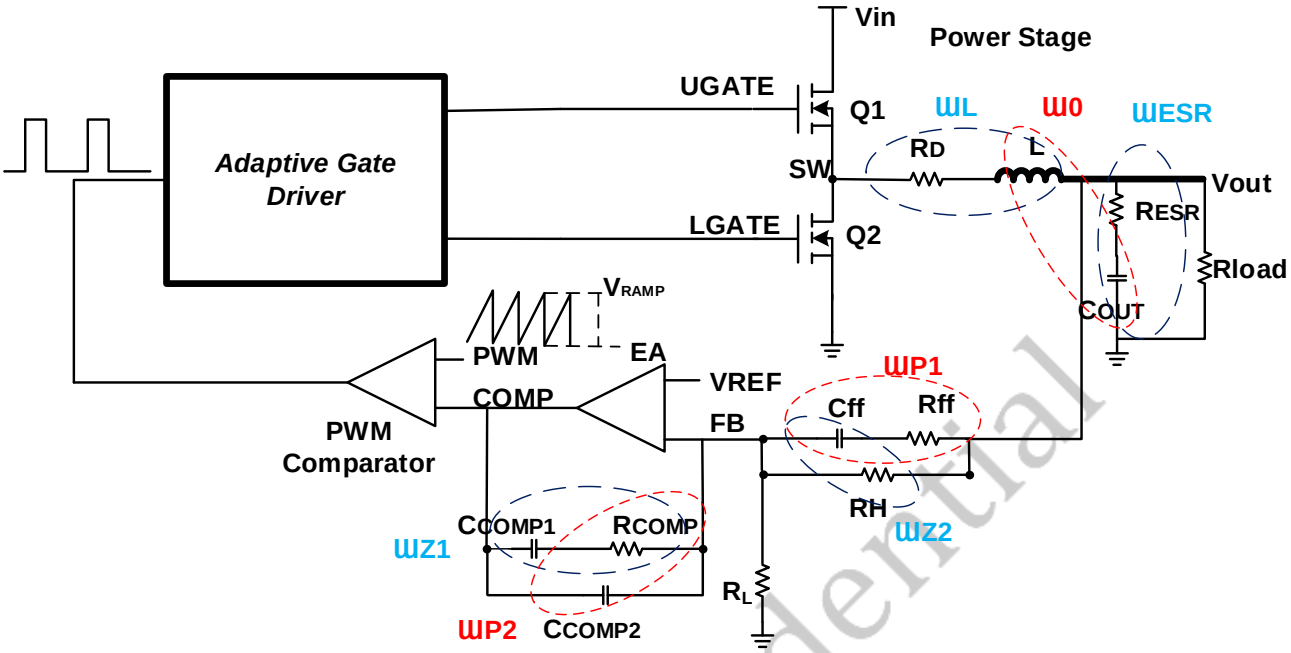
• Output charge, Q_{OSS}, at the relevant input voltage;

• Body diode reverse recovery charge, Q_{RR};

• Gate threshold voltage, $V_{GS(th)}$, derived from the plateau in the Q_G vs. V_{GS} plot in the MOSFET data sheet. With a MOSFET Miller plateau voltage typically in the range of 3 V to 5 V, the 7.5-V gate drive amplitude of the JWH6346 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

Control Loop Compensation

The poles and zeros inherent to the power stage and compensator are respectively illustrated by red and blue dashed rings in the schematic embedded in Table 1. The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, RL, has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature.



POWER STAGE POLES	POWER STAGE ZEROS	COMPENSATOR POLES	COMPENSATOR ZEROS
$\omega_0 = \frac{1}{\sqrt{L * C_{OUT}\left(\frac{1+{R_{ESR}}/{R_{load}}}{1+{R_{ESR}}/{R_D}}\right)}} \approx \frac{1}{\sqrt{L * C_{OUT}}}$	$\omega_{ESR} = \frac{1}{R_{ESR} * C_{OUT}}$	$\omega_{P1} = \frac{1}{R_{ff} * C_{ff}}$	$\omega_{Z1} = \frac{1}{R_{COMP} * C_{COMP1}}$
	$\omega_L = \frac{L}{R_D}$	$\omega_{P2} = \frac{1}{R_{COMP} * (C_{COMP1} // C_{COMP2})}$	$\omega_{Z2} = \frac{1}{(R_H + R_{ff}) * C_{ff}}$

Table1: Buck Regulator Poles and Zero

Note: RESR represents the ESR of the output capacitor COUT.
$R_D = D * R_{dsonUgate} + (1-D) * R_{dsonLgate} + R_{DCR}$, shown as a lumped element in the schematic, represents the effective series damping resistance.

The small-signal open-loop response of a buck regulator is the product of modulator, power train and compensator transfer functions. The power stage transfer function can be represented as a complex pole pair associated with the output LC filter and a zero related to the ESR of the output capacitor. The DC (and low frequency) gain of the modulator and power stage is VIN/VRAMP. The gain from COMP to the average voltage at the input of the LC filter is held essentially constant by the PWM line feedforward feature of the JWH6346 (15 V/V or 23.5 dB).

Complete expressions for small-signal frequency analysis are presented in Table 2. The transfer functions are denoted in normalized form. While the loop gain is of primary importance, a regulator is not specified

directly by its loop gain but by its performance related characteristics, namely closed-loop output impedance and audio susceptibility.

TRANSFER FUNCTION	EXPRESSION
Open-loop transfer function	$T_V(S)=\frac{v_{comp}(S)}{v_o(S)}*\frac{v_o(S)}{d(s)}*\frac{d(s)}{v_{comp}(S)}=G_C(S)*G_{VD}(S)*F_M$
Duty-cycle-to-output transfer function	$G_{VD}(S)=\frac{v_o(S)}{d(s)}\|vin(S)=0;iO(S)=0=V_{IN}*\frac{1+\frac{S}{\omega_{ESR}}}{1+\frac{S}{Q_0*\omega_0}+\frac{S^2}{{\omega_0}^2}}$
Compensator transfer function	$G_C(S)=\frac{v_{comp}(S)}{v_o(S)}=Kmid*\frac{\left(1+\frac{\omega_{Z1}}{S}\right)*\left(1+\frac{S}{\omega_{Z2}}\right)}{\left(1+\frac{S}{\omega_{P1}}\right)*\left(1+\frac{S}{\omega_{P2}}\right)}$
Modulator transfer function	$F_M=\frac{d(s)}{v_{comp}(S)}=\frac{1}{V_{RAM}}$

Table2: Buck Regulator Small-Signal Analysis

Note: Kmid = RCOMP1/RH is the mid-band gain of the compensator. By expressing one of the compensator zeros in inverted zero format, the midband gain is denoted explicitly.

If the pole located at ωp1 cancels the zero located at ωESR and the pole at ωp2 is located well above crossover, the expression for the loop gain, Tv(s) in Table 2, can be manipulated to yield the simplified expression given in below Equation.

$$T_V(S)=R_{COMP}*C_{ff}*\frac{V_{IN}}{V_{RAMP}}*\frac{{\omega_0}^2}{S}$$

Essentially, a multi-order system is reduced to a single-order approximation by judicious choice of compensator components. The crossover frequency can be calculate by below Equation

$$\omega_c=2*\pi*f_c=\omega_0*Kmid*\frac{V_{IN}}{V_{RAM}}$$

$$Kmid=\frac{f_c}{f_0}*\frac{1}{K_{FF}}=\frac{R_{COMP}}{R_H}$$

The loop crossover frequency is usually selected between one-tenth to one-fifth of switching frequency. Inserting an appropriate crossover frequency into Equation Wc gives a target for the mid-band gain of the compensator, Kmid. Given an initial value for RH, RH is then selected based on the desired output voltage. Values for RCOMP, Rff, CCOMP1, CCOMP1 and Cff are calculated from the design expressions listed in Table 3, with the premise that the compensator poles and zeros are set as follows: Wz1 = 0.5·Wo, Wz2 = Wo, Wp1 =WESR, Wp2 = WSW/2.

RESISTORS	CAPACITORS
$R_L=\frac{R_H}{\left(\frac{V_{OUT}}{0.8}-1\right)}$	$C_{COMP1}=\frac{2}{\omega_0*R_{COMP}}$
$R_{COMP}=\ Kmid*R_H$	$C_{COMP2}=\frac{1}{\omega_{P2}*R_{COMP}}$
$R_{ff}=\frac{1}{\omega_{P1}*C_{ff}}$	$C_{ff}=\frac{1}{\omega_{Z2}*R_H}$

Table3: Compensation Component Selection

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JWH6346 (VIN pin and GND pin) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. Keep the switching node SW short to

prevent excessive capacitive coupling

4. Make Vin, Vout and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

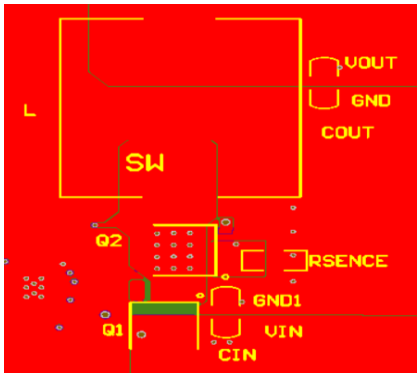


Figure 18. Top Layer

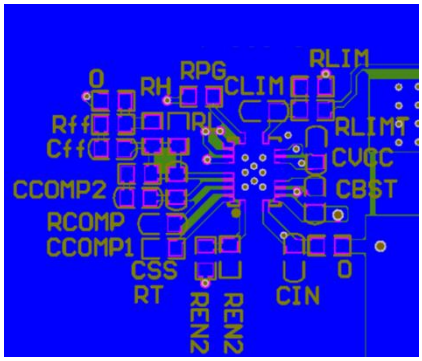


Figure 19. Bottom Layer

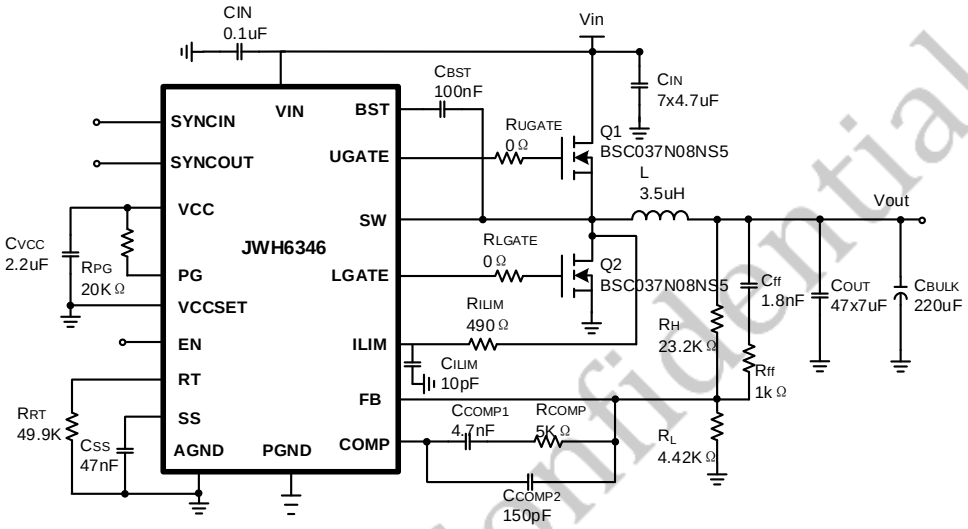
REFERENCE DESIGN

V_{IN}: 7V~75V

V_{OUT}: 5V

Frequency: 200kHz

I_{OUT}: 0~20A



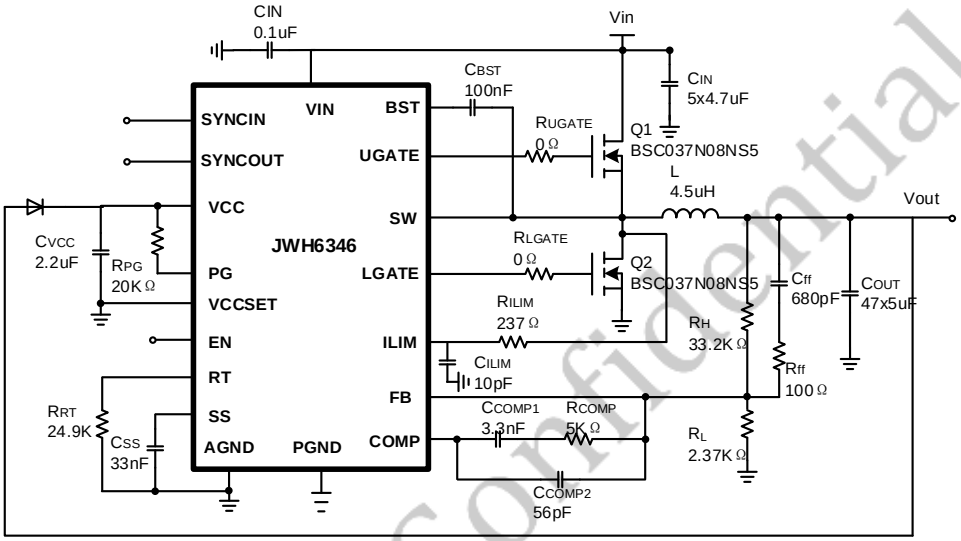
REFERENCE DESIGN

V_{IN}: 15V~100V

V_{OUT}: 12V

Frequency: 400kHz

I_{OUT}: 0~10A



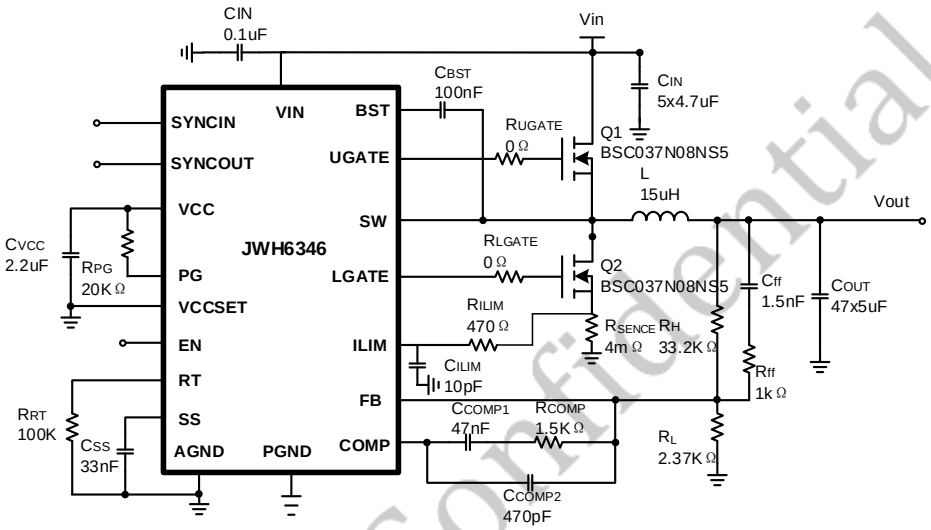
REFERENCE DESIGN

V_{IN}: 15V~75V

V_{OUT}: 12V

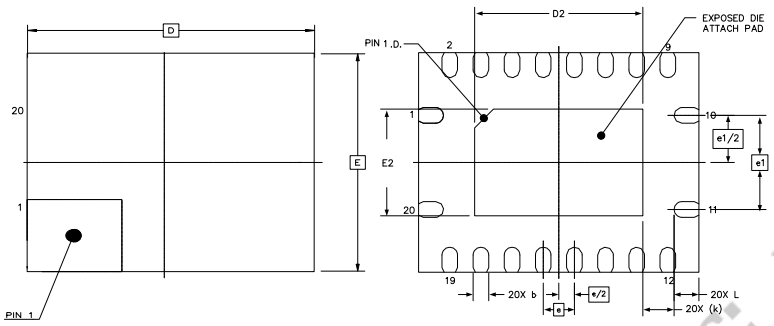
Frequency: 100kHz

I_{OUT}: 0~10A

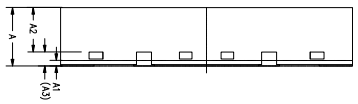


PACKAGE OUTLINE

QFN3.5X4.5-20 UNIT: mm

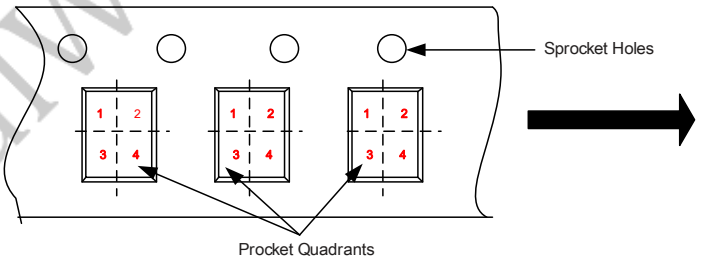


SYMBOL	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	---	0.65	---
A3		0.203 REF	
b	0.2	0.25	0.3
D		4.5 BSC	
E		3.5 BSC	
e		0.5 BSC	
e1		1.5 BSC	
D2	2.6	2.7	2.8
E2	1.6	1.7	1.8
L	0.3	0.4	0.5
K		0.5 REF	



SIDE VIEW

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN3.5X4.5-20	1

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