# JW1566BD

## Offline QR GaN Flyback Converter

*Preliminary Specifications Subject to Change without Notice*

## DESCRIPTION

The JW1566BD is an isolated offline Flyback converter with GaN integrated, which features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and benefits EMI performance with nature frequency variation. And an internal frequency limitation is utilized to overcome the inherent disadvantages of QR Flyback.

The JW1566BD comprises a HV pin for startup to eliminate conventional startup resistor and save standby mode energy consumption.

The JW1566BD is available in PVDFN5X6-8 package. The high level of integration provides an easy-to-use, low component count and high efficiency application solution for isolated power delivery.



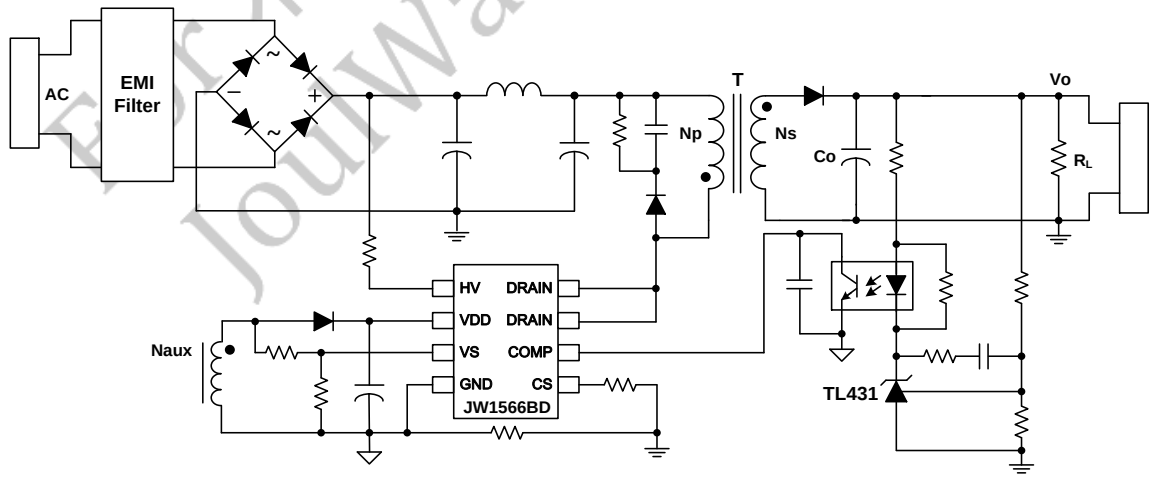
## FEATURES

- Integrated 650V GaN
- Built-in High-Voltage Startup
- Wider VDD Operation Range
- QR Operation for High Efficiency
- Optional OCP and OPP Function for Different PD and QC Output Application
- Very Low Standby Power Consumption
- Cycle-by-Cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP, Brown-In, Brown-out, CS Open Protection, OCP, OPP, OLP, Internal OTP
- Frequency Jitter to Ease EMI Compliance
- PVDFN5X6-8 Package

## APPLICATIONS

- PD and QC Chargers
- AC/DC Adapters with Wide Output Range

## TYPICAL APPLICATION



## ORDER INFORMATION

| DEVICE[1)] | PACKAGE | TOP MARKING[2)] | ENVIRONMENTAL[3)] |
|---|---|---|---|
| JW1566BDPVDLQF#TR | PVDFN5X6-8 | JW1566BD<br>YW□□□□□ | Green |

**Notes:**

1) JW□ □ #TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

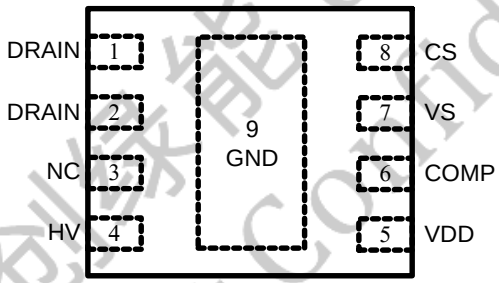
2) Line1: JW □□□□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

## PIN CONFIGURATION

TOP VIEW




PVDFN5X6-8

## ABSOLUTE MAXIMUM RATING[1)]

HV Voltage ..... 700V
DRAIN Pin ..... 650V
VDD Pin ..... 95V
COMP, CS Pin .....-0.3V to 5V (-0.75V to -0.3V<10us, 5V to 5.5V<10us)
VS Pin ..... -0.3V to 5V (-0.75V to -0.3<10us, 5V to 5.5V<10us)
Junction Temperature[2)] ..... 150ºC
Storage Temperature ..... -65ºC to 150ºC
Lead Temperature (Soldering, 10sec.) ..... 260ºC

## RECOMMENDED OPERATING CONDITIONS [3)]

VDD Voltage ..... 8V to 83V
Operating Junction Temperature ($T_J$) ..... -40ºC to 125ºC

## THERMAL PERFORMANCE[4)]

| | $\theta_{JA}$ | $\theta_{Jc}$ |
|---|---|---|
| PVDFN5X6-8 | TBD | TBD |

**Note:**

**1)** Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

**2)** The JW1566BD includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

**3)** The device is not guaranteed to function outside of its operating conditions.

**4)** Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

*$T_A$ = 25ºC, unless otherwise stated.*

*Advance Information, not production data, subject to change without notice.*

| ITEM | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| ***High Voltage Section (HV Pin)*** | | | | | | |
| Supply Current from HV Pin | $I_{HV}$ | $V_{HV}$=120V, $V_{VDD}$=0V | 2.5 | 3 | 3.5 | mA |
| Leakage Current of HV Pin | $I_{HV\_LK}$ | $V_{HV}$=500V, $V_{VDD}$=20V | | 20 | 30 | uA |
| Brown-In Threshold | $V_{BR\_IN}$ | $V_{HV}$ increasing | 106 | 112 | 118 | V |
| Brown-Out Threshold | $V_{BR\_OUT}$ | $V_{HV}$ decreasing | 91 | 97 | 103 | V |
| Brown-Out Blanking Time[6)] | $t_{BR\_OUT}$ | | | 70 | | ms |
| ***Supply Voltage Section (VDD Pin)*** | | | | | | |
| Turn-On Threshold Voltage | $V_{DD\_ON}$ | $V_{VDD}$ increasing | 15 | 16.5 | 18 | V |
| Turn-Off Threshold Voltage | $V_{DD\_OFF}$ | $V_{VDD}$ decreasing | 6.8 | 7.7 | 8.6 | V |
| Reset Threshold Voltage | $V_{DD\_RST}$ | Fault State | 3.9 | 4.75 | 5.6 | V |
| Startup Current | $I_{DD\_ST}$ | $V_{VDD}$=$V_{DD\_ON}$-0.5 V | 240 | 280 | 320 | uA |
| Operating Supply Current | $I_{DD\_OP}$ | $V_{VDD}$=20V, $f_S$=$f_{max}$ | 0.5 | 0.7 | 1 | uA |
| VDD OVP Voltage | $V_{DD\_OVP}$ | $V_{VDD}$ increasing | 85 | 90 | 94.5 | V |
| ***Voltage Sense Section (VS Pin)*** | | | | | | |
| Maximum VS Source Current Capability | $I_{VS\_MAX}$ | $V_{VS}$=-0.4V | 2.5 | 3 | 3.5 | mA |
| Adaptive Blanking Time for VS Sampling[6)] | $t_{VS\_BLK}$ | $V_{COMP}$=0.55V | | 0.6 | | us |
| | | $V_{COMP}$=4V | | 1.2 | | us |
| Output OVP Threshold | $V_{VS\_OVP}$ | $V_{VS}$ increasing | 2.8 | 3 | 3.2 | V |
| Output OVP Debounce Cycle Counts[6)] | $N_{VS\_OVP}$ | Fault State | | 3 | | Cycle |
| ***Current Sense Section (CS Pin)*** | | | | | | |
| Max CS Offset Current | $I_{CS\_MAX}$ | $V_{COMP}$=4V | 95 | 100 | 105 | uA |
| Min CS Offset Current | $I_{CS\_MIN}$ | $V_{COMP}$=0V at Burst Mode | 20 | 27.5 | 35 | uA |
| CS Off Threshold | $V_{CS\_TH}$ | $V_{CS}$ decreasing | -30 | 0 | 30 | mV |
| Leading-Edge Blanking Time[6)] | $t_{LEB}$ | $V_{CS}$=0 | | 220 | | ns |
| OCP Enable Threshold | $V_{OCP\_EN}$ | | 0.58 | 0.67 | 0.76 | V |
| OCP Internal Threshold[6)] | $V_{OCP}$ | | | 0.2 | | V |
| OCP Blanking Time | $t_{OCP\_BLK}$ | Fault State | 85 | 105 | 125 | ms |
| Auto-Restart Cycles for OCP[6)] | $N_{OCP\_HIC}$ | Fault State | | 4 | | Cycle |
| ***Frequency Section*** | | | | | | |
| Maximum Switching Frequency | $f_{max}$ | $V_{COMP}$=3.5V | 80 | 115 | 150 | kHz |
| Minimum Switching Frequency | $f_{min}$ | $V_{COMP}$=0.8V | 20 | 25 | 30 | kHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| Maximum ON Time | $T_{ON\_MAX}$ | | 15.5 | 19 | 22.5 | us |
| Minimum ON Time | $T_{ON\_MIN}$ | | 230 | 280 | 330 | ns |
| Maximum Switching Cycle | $T_{S\_MAX}$ | | 48 | 58 | 68 | us |
| Frequency Jittering Amplitude to COMP[6)] | $\Delta F_{JIT}$ | | | ±7% | | |
| Counting Cycles for Jittering[6)] | $N_{JIT\_CYC}$ | | | 32 | | Cycle |
| ***Feedback Section (COMP Pin)*** | | | | | | |
| Open Pin Voltage[6)] | $V_{COMP\_MAX}$ | Open Loop | | 4 | | V |
| Internal Pull-Up Resistor[6)] | $R_{COMP\_UP}$ | | | 20 | | kΩ |
| COMP to CS Offset Current Gain[6)] | $G_{COMP\_CS}$ | COMP > 2.8V | | 20 | | V/mA |
| | | COMP < 1.0V | | 16 | | V/mA |
| The Threshold Enter PFM Mode | $V_{COMP\_PFM}$ | $V_{COMP}$ decreasing | 2.6 | 2.8 | 3 | V |
| The Threshold Enter Burst Mode | $V_{BUR\_L}$ | $V_{COMP}$ decreasing | 0.43 | 0.51 | 0.59 | V |
| The Threshold Exit Burst Mode | $V_{BUR\_H}$ | $V_{COMP}$ increasing | 0.52 | 0.6 | 0.68 | V |
| OPP Internal Threshold[6)] | $V_{OPP}$ | | | 0.8 | | V |
| OPP Blanking Time | $t_{OPP\_BLK}$ | Fault State | 85 | 105 | 125 | ms |
| Auto-Restart Cycles for OPP[6)] | $N_{OPP\_HIC}$ | Fault State | | 4 | | Cycle |
| Over Load Protection Threshold[6)] | $V_{OLP}$ | Fault State | | 3.7 | | V |
| OLP Blanking Time[6)] | $t_{OLP\_BLK}$ | Fault State | 85 | 105 | 125 | ms |
| Auto-Restart Cycles for OLP[6)] | $N_{OLP\_HIC}$ | Fault State | | 4 | | Cycle |
| ***GaN Section*** | | | | | | |
| Drain-source On-state Resistance | $R_{DS\_ON}$ | Ta=25℃ | | 620 | 1000 | mΩ |
| ***Internal Over Temperature Protection*** | | | | | | |
| Thermal Shutdown Threshold[6)] | $T_{OTP}$ | Internal junction temperature | | 140 | | °C |
| OTP Hysteresis[6)] | $T_{HYS}$ | Internal junction temperature | | 30 | | ºC |

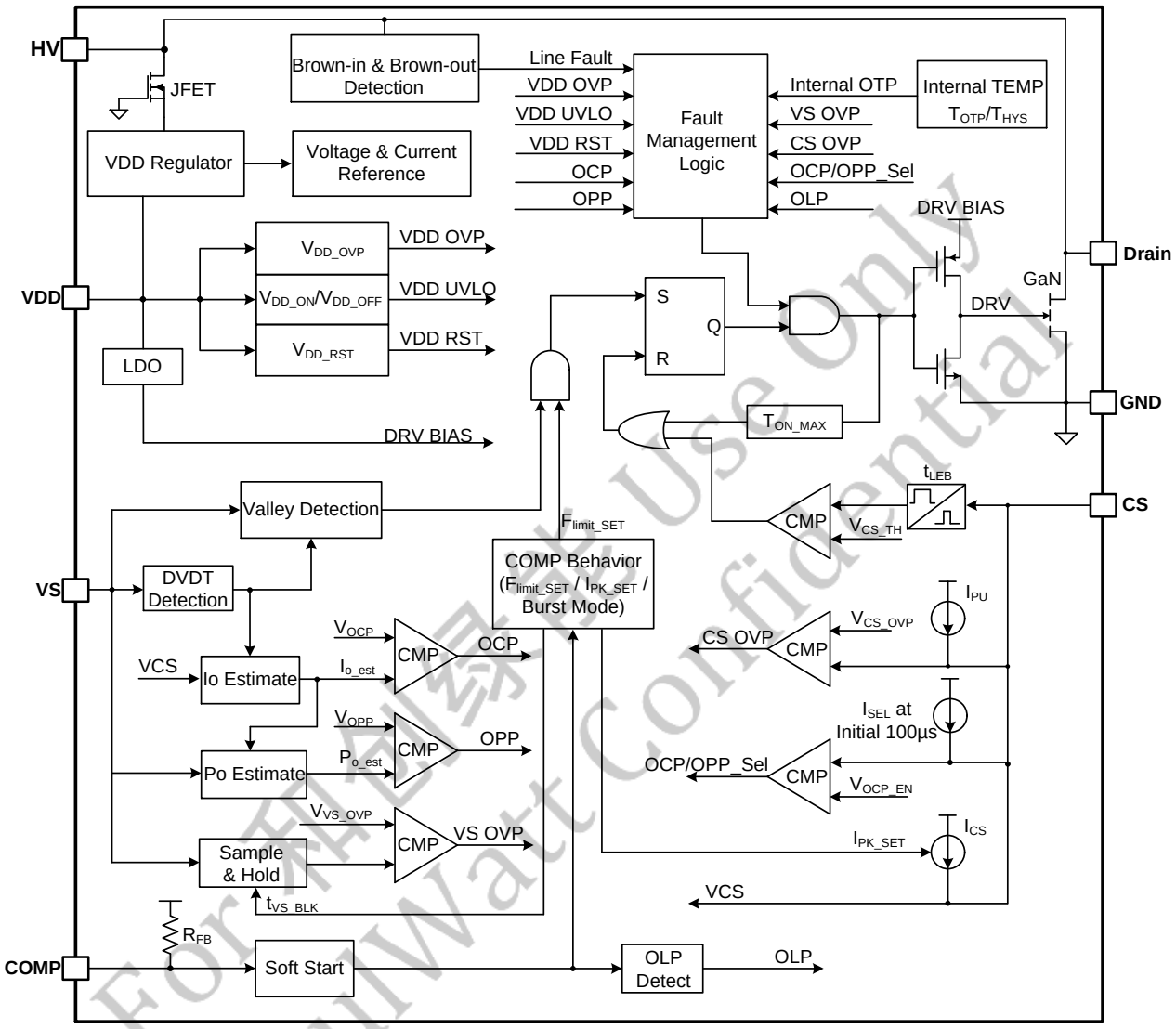
## Note:

**6)** Guaranteed by design.

## PIN DESCRIPTION

| PIN PVDFN5X6-8 | NAME | DESCRIPTION |
|---|---|---|
| 1, 2 | DRAIN | Drain terminal of the Internal GaN. |
| 3 | NC | |
| 4 | HV | High voltage input pin. This pin provides source current to charge VDD. This pin also senses input voltage for brown-in and brown-out protection. |
| 5 | VDD | Bias power input to the controller. A hold-up capacitor to GND is required. |
| 6 | COMP | Feedback input pin for Flyback QR controller. Connect to an opto-coupler. |
| 7 | VS | Voltage sensing input pin. Coupled to the auxiliary winding via a resistor divider to monitor the output voltage for OVP protection. This pin also detects the resonant valley to implement QR operation. |
| 8 | CS | Current sensing input pin. This pin sense the primary switch current for peak current control and OCP. Besides, this pin is used to choose OCP or OPP function at the initial start. |
| 9 | GND | The ground of IC. |

## BLOCK DIAGRAM



# FUNCTIONAL DESCRIPTION

The JW1566BD is an offline flyback converter with GaN intergrated, which features multi-mode quasi-resonant (QR) operation. The Quasi-Resonant (QR) with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

JW1566BD has an inherent frequency jittering mechanism to improve EMI performance under QR operation.

## 1. Start-Up

### 1.1. HV Start-Up

When HV is connected to the input bulk capacitor, the internal JFET turns on and a HV current source starts to charge VDD cap. As soon as VDD reaches turn-on threshold $V_{DD\_ON}$, the internal startup circuit is disabled. The controller is enabled and the converter starts switching.

### 1.2 Soft-Start

In the absence of a detected fault, the converter begins to work normally along with soft start. The internal soft-start time is within 4ms with the feedback signal $V_{COMP}$ rising gradually from minimum level to maximum level. Every restart up is followed by a soft start.

## 2. Normal Operation

After the converter start-up, it enters normal operation. The JW1566BD realizes output adjustment based on the feedback signal transmitting to the primary-side controller by the opto-coupler.

The JW1566BD is a multi-mode QR converter with secondary-side regulation. According to the feedback signal $V_{COMP}$, the converter operates in different modes for efficiency optimization. Fig.1 illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in Fig.1.

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to $f_{max}$. For medium-load range, the Pulse Frequency Modulation (PFM) is used and primary peak current is nearly fixed to achieve high efficiency. When the load is further reduced, switching frequency is fixed at $f_{min}$ along with primary peak current varying from 50% to 25% of its maximum. When the system is at very light load condition, the control mode of JW1566BD changes to burst mode. When the voltage of COMP pin drops below $V_{BUR\_L}$ (0.5V typically), the drive stops. The drive will resume when the voltage of COMP pin rises back to $V_{BUR\_H}$ (0.6V typically). Otherwise, the internal GaN remains at off state to minimize the switching loss and reduce the standby power consumption. Transitions between modes are automatically accomplished by the controller depending on the feedback signal, $V_{COMP}$.

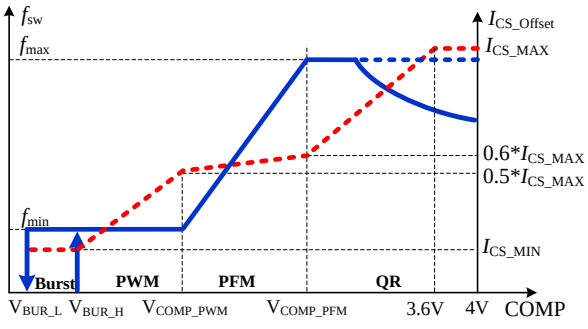



Fig.1 Frequency & Ipk Modulation

## 3. Other Functions and Features

### 3.1 Frequency Jittering

To achieve good EMI performance, frequency jittering method is integrated in JW1566BD. The frequency jittering is achieved by varying the switching frequency directly. The variation is ±7% around its normal value. The modulation cycle is determined by counting consecutive 32 switching cycles.

### 3.2 Lead Edge Blanking (LEB)

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between the CS pin and the current comparator input. The current comparator is disabled and can't turn off the internal GaN during the blanking time. Fig.2 shows the leading edge blanking time.

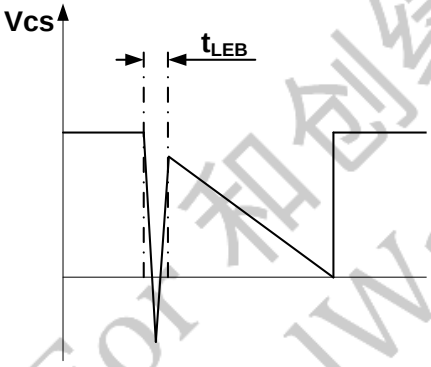



Fig.2 LEB Blanking

### 3.3 CCM Preventing

For JW1566BD, when the primary-side peak current exceeds the value decided by the feedback signal $V_{COMP}$, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after a $T_{S\_MAX}$ to make sure the system operates in DCM.

### 3.4 VS Blanking Time

VS spikes are affected by the amplitudes of Ipk and inductance, so VS blanking time should be set to vary with Ipk. Ensure that the secondary side conduction time is greater than the VS blanking time $t_{BLK}$.

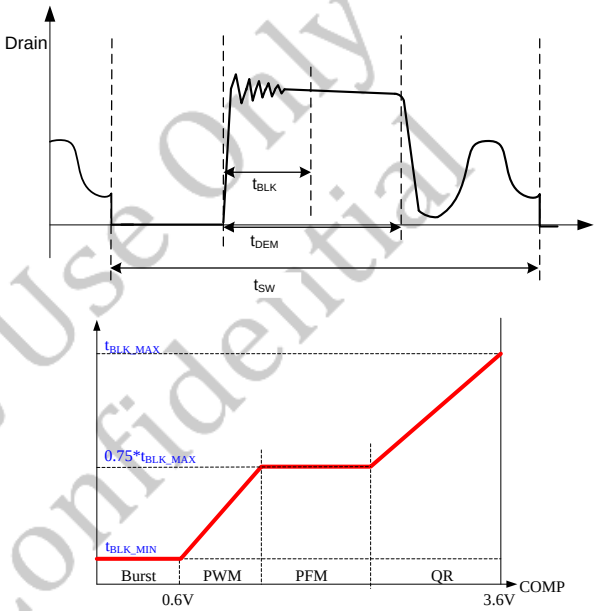



Fig.3 VS Blanking Time

## 4. Protection

### 4.1 CS Pin Open Protection

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin, increasing the $V_{CS}$. If $V_{CS}$ is above $V_{CS\_OVP}$ (2V typically), a CS pin open fault triggered.

### 4.2 Input Brown-in and Brown-out

The JW1566BD senses HV voltage to realize brown in function. When HV voltage is higher than $V_{BR\_IN}$ (112V typically), a 5mA pull down current will be applied to VDD pin to make VDD hit $V_{DD\_OFF}$. When VDD reaches $V_{DD\_ON}$ again, the controller starts switching.

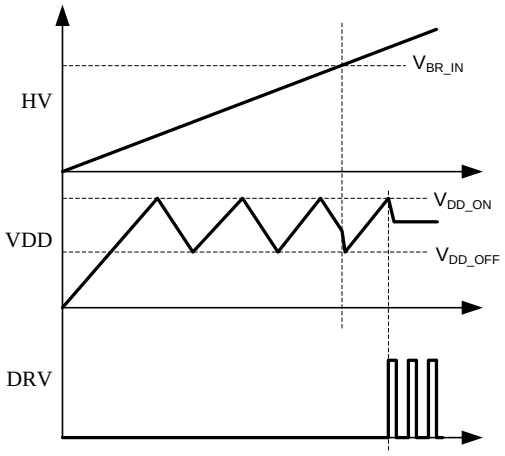



Fig.4 Brown-In at Drain Terminal

And the controller is disabled when HV voltage is lower than $V_{BR\_OUT}$ (98V typically) for brown-out blanking time (70ms typically). The blanking time is set long enough to ignore a two cycle drop out. The timer starts counting once HV voltage drops below $V_{BR\_OUT}$.

### 4.3 Output OVP (VS OVP)

The output over voltage protection is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds $V_{VS\_OVP}$ for three consecutive switching cycles, an VS_OVP fault is asserted, and then the device shuts down, the UVLO reset and re-start fault cycle begins.

### 4.4 OCP or OPP Selection Circuit

In some PD or QC applications, the maximum output current at different output voltage differs much. So OCP should be disabled, and the alternative OPP is enabled. JW1566BD senses CS voltage at initial start to determine whether to use OCP or OPP function as Fig.5 shows. At the initial 100us, an OCP/OPP selection current $I_{SEL}$ (100uA, typically) is applied to CS pin. If CS voltage exceeds a preset enable threshold $V_{OCP\_EN}$, OPP is enabled and OCP is disabled. Otherwise, OPP is disabled and OCP is enabled.

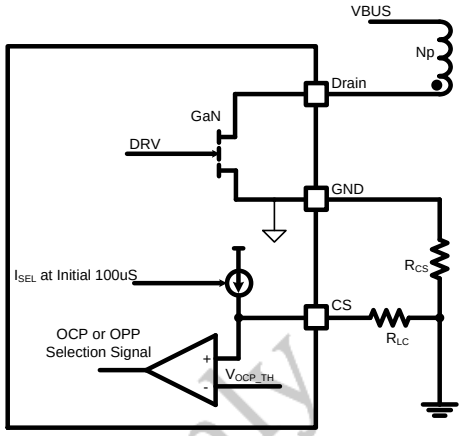



Fig.5 OCP or OPP Selection Circuit

### 4.5 OCP

If OCP is enabled, JW1566BD compares estimated output average current and OCP threshold. The output average current is calculated at the primary side. When the primary switch turns off, the peak inductor current $I_{pk}$ is sampled and hold for output current calculation.

As shown in Fig.6, it calculates output current based on secondary side current conduction time $t_{ons}$ and primary side current information $V_{CS}$. If the calculated output current signal, $I_{o\_est}$ is higher than the internal OCP threshold $V_{OCP}$ (0.2V typically) for an OCP blanking time $t_{OCP\_BLK}$, IC enters OCP protection.

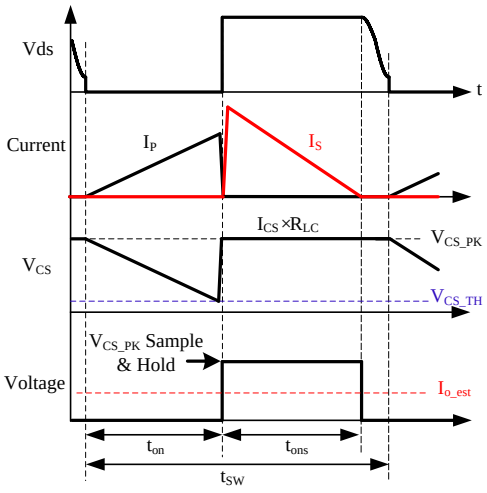



Fig.6 Output Current Estimation

So, the OCP point can be set as:

$$I_{OCP} = \frac{V_{OCP} \cdot \left(1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}\right)}{2R_{CS}} \cdot \frac{N_P}{N_S} \quad (1)$$

wherein, $N_P$ is the turns number of primary winding, $N_S$ is the turns number of secondary winding, $R_{cs}$ is the current sensing resistance.

When an OCP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit $V_{DD\_OFF}$ four times, and then the device restarts at the fifth cycle.

### 4.6 OPP

If OPP is enabled, JW1566BD compares estimated output power and OPP threshold. The output power is calculated at the primary side based on the estimated output average current in OCP and the output voltage according to VS voltage. So the output power can be expressed as:

$$P_{o\_est} = \frac{V_{CS\_PK} - V_{CS\_TH}}{2R_{CS}} \cdot \frac{N_P}{N_S} \cdot \frac{t_{ons}}{t_{SW}} \cdot \frac{V_S \cdot N_S}{N_{aux}} \cdot \frac{R_{DOWN} + R_{UP}}{R_{DOWN}} \quad (2)$$

And the OPP point can be set as:

$$P_{OPP} = \frac{V_{OPP} \cdot \left(1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}\right)}{2R_{CS}} \cdot \frac{N_P}{N_{aux}} \cdot \frac{R_{DOWN} + R_{UP}}{R_{DOWN}} \quad (3)$$

wherein, $N_{aux}$ is the turns number of auxiliary winding, $N_P$ is the turns number of primary winding, $R_{UP}$ and $R_{DOWN}$ are the resistances of the outside resistor divider of VS pin.

If the calculated output power signal is higher than the internal OPP threshold $V_{OPP}$ (0.8V typically) for an OPP blanking timer $t_{OPP\_BLK}$, IC enters OPP protection. When an OPP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit $V_{DD\_OFF}$ four times, and then the device restarts at the fifth cycle.

### 4.7 Over Load Protection

If the voltage on COMP pin continues exceeds the Over-Load protection threshold (3.7V typically) more than an OLP blanking time $t_{OLP\_BLK}$, an OLP fault is asserted. The device shuts down, VDD needs to hit $V_{DD\_OFF}$ four times, and then the device restarts at the fifth cycle..

### 4.8 VDD OVP

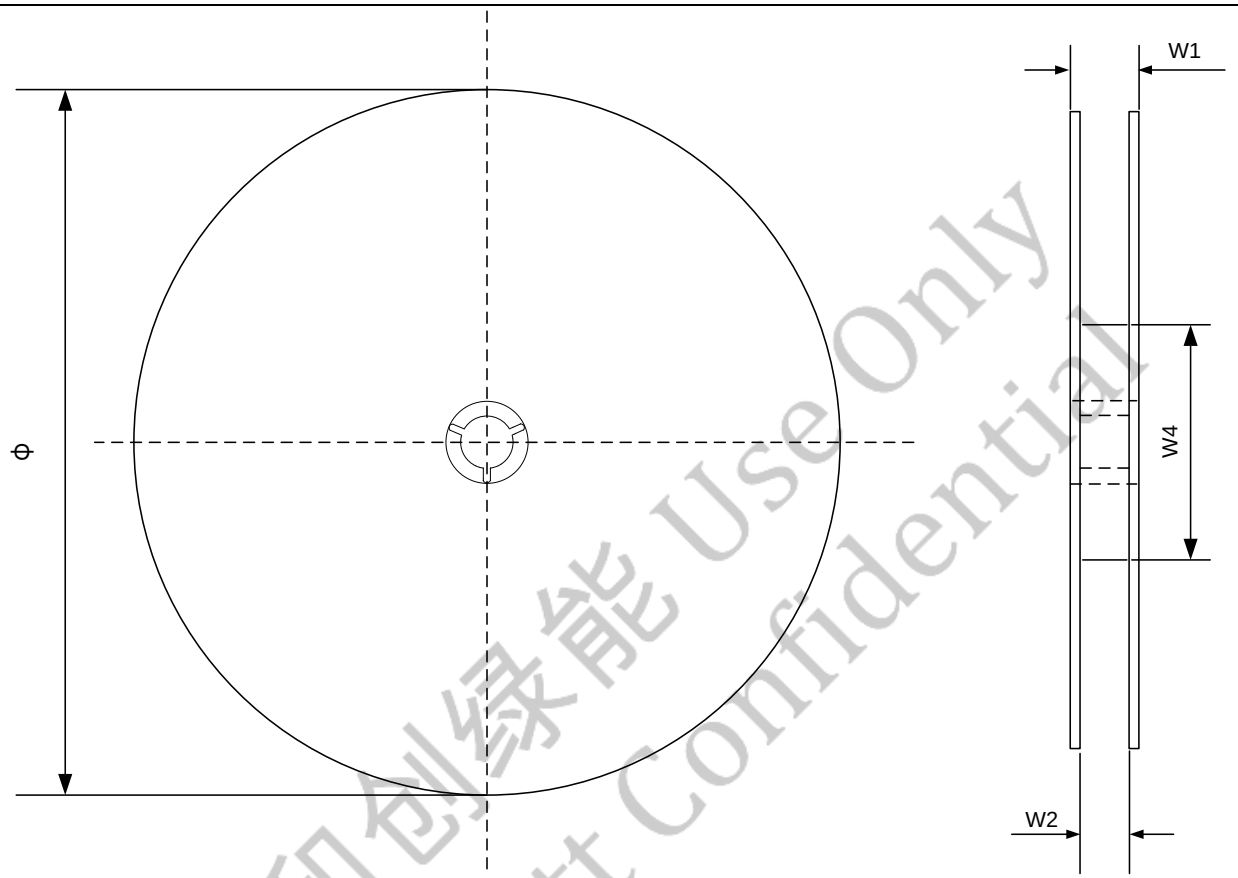
If the voltage on VDD pin continues exceeds the Over-Voltage protection threshold $V_{DD\_OVP}$ (90V typically) more than 100us, a VDD_OVP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

### 4.9 Internal OTP

The internal over temperature protection threshold is $T_{OTP}$ (140°C typically). If the junction temperature of the device reaches this threshold, the device shuts down. Since the OTP hysteresis is 30°C typically, when the junction temperature falls below 110°C, the device initiates the UVLO reset and re-starts fault cycle.

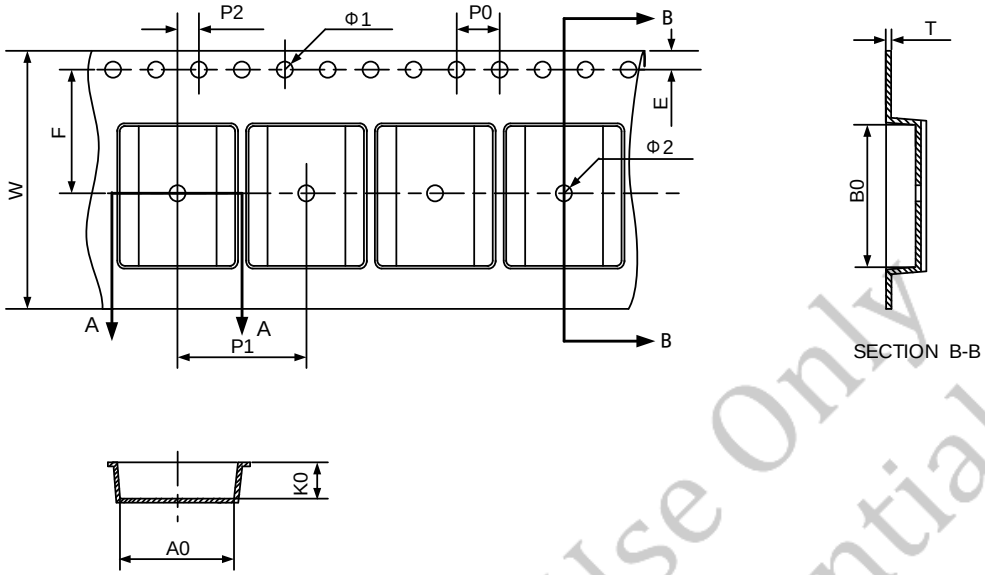
## TAPE AND REEL INFORMATION

Reel UNIT: mm




| Package | Diameter Φ | Thickness W1 | Width W2 | W4 |
|---|---|---|---|---|
| PVDFN5x6-8 | 330±2 | 17.6±2 | 12.4±2 | 100±2 |

Carrier Tape UNIT: mm



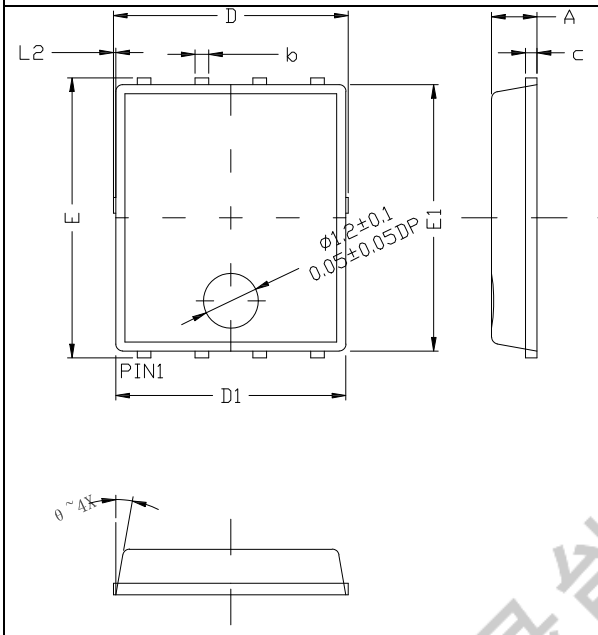

Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

| Package | Tape dimensions (mm） | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | P0 | P2 | P1 | A0 | B0 | W | T | K0 | Φ1 | Φ2 | E | F |
| PVDFN5x6-8 | 4.0±0.1 | 2.0±0.1 | 8.00±0.10 | 6.40±0.2 | 5.42±0.2 | 12.0±0.3 | 0.2±0.1 | 1.25±0.2 | 1.50min | 1.50min | 1.75±0.1 | 5.50±0.10 |

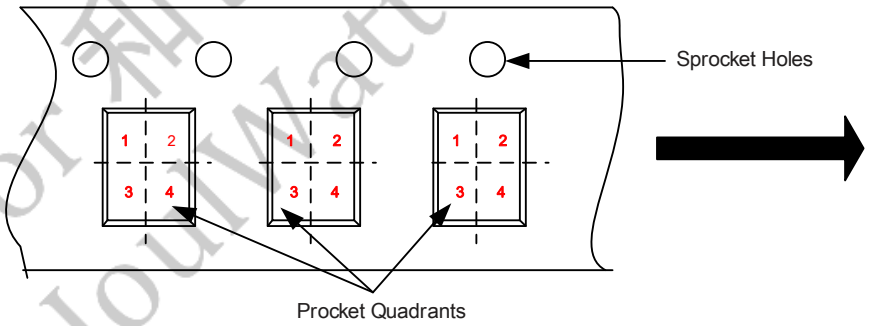
## PACKAGE OUTLINE

PVDFN5X6-8 UNIT: mm




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.25 | 0.30 | 0.35 |
| b1 | 0.30 | 0.40 | 0.45 |
| c | 0.22 | 0.25 | 0.28 |
| D | -- | -- | 5.30 |
| D1 | 4.90 | 5.05 | 5.20 |
| D2 | 4.10 REF | | |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.85 | 6.00 |
| E2 | 2.35 REF | | |
| e | 1.10 | 1.27 | 1.40 |
| H | 0.51 | 0.61 | 0.71 |
| K | 1.00 REF | | |
| K1 | 1.50 REF | | |
| L | 0.51 | 0.61 | 0.71 |
| L2 | -- | -- | 0.10 |
| θ | 8° | ~ | 12° |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE**




| Package Type | Pin1 Quadrant |
|---|---|
| PVDFN5X6-8 | 1 |

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